EEE 311/312 Lab
Textbook

ELECTRONIC EXPERIMENTS

A TEXT-LAB MANUAL

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to our

parents

and

families

CONTENTS

PREFACE

This laboratory manual is prepared for the students taking the third year electronics courses offered in the Electrical and Electronics Engineering Department at the University of Gaziantep. Although the measuring instruments and the devices used in the experiments are those available in the Electronics Laboratory of the Electrical and Electronics Engineering Department of the University of Gaziantep, the experiments can be performed in any laboratory having similar facilities. The content is designed according to the present facilities in the Electronics Laboratory. The content covers the course material of the courses EEE311 and EEE312 at the University of Gaziantep.

The manual is mainly intended to verify in the laboratory the theory taught in the Electronics courses mentioned above. However, basic theory is also given before each experiment to familirize students with the experiment even if the content of the experiment is not fully covered in the course. The text is divided into four sections as follows:

Chapter 1 introduces the laboratory regulations, safety precautions, remarks on presenting laboratory notebooks and on using the laboratory instruments effectively.

Chapter 2 includes descriptions and operating instructions of the equipment to be used in the experiments.

Chapter 3 is devoted to the experiments. It contains a total of 17 experiments which the first one is an introduction to the instruments used

in the laboratory. It is recommended by the authors that the experiments 1 to 9 are performed in the first semester and 10 to 17 in the second semester.

Chapter 4 includes the data sheets for the parts used in the experiments. In addition to the general specifications of these parts, case and pin diagrams are also given in this chapter.

Each experiment is divided into five parts. "Objective" gives the purpose of the experiment to be performed. The complementary information about the theory related to the experiment is given under the heading "Theory". "Preliminary" involves the detailed analysis of the experiment and must be completed before coming to the laboratory. "Experimental Procedure" gives the steps to be followed during the experiment. "Conclusion" is included for the evaluation of the experiment, significance of the results, and for a discussion of the differences between the theoretical and experimental results.

The authors express their thanks to Nuran Doğru and Ulus Çevik for their comments. Special thanks go to Halil Gerez for valuable drawings.

November 1997, Gaziantep

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CHAPTER 1

GENERAL LABORATORY RULES

LABORATORY REGULATIONS

The students must follow the following regulations in order the laboratory work to be done properly without any trouble or interruption:

1) Experiments will be performed in pairs. Everybody has to choose a partner to perform the experiments together. Each pair will be given a table number. Nobody can change his/her partner unless the assistants are informed.

2) No visitors are permitted in the laboratory.

3) There should be no loud talking in the laboratory.

4) The transfer of any equipment between the tables by the students is strictly forbidden. If an instrument misoperates, inform the assistants or technicians so that they can supply you another one.

5) Before leaving the laboratory, arrange everything you have used on your table in the form that you have found them when you come to the laboratory.

6) You will not be allowed to perform the experiment unless you prepare the preliminary work before coming to the laboratory.

SAFETY PRECAUTIONS

In order to perform the experiments safely, avoiding any personal danger or injury and any damage of the instruments, the following should always be kept in mind:

1) Read the related part of the laboratory manual thoroughly before coming to the laboratory and pay attention to all instructions before and during the experiment.

2) Always disconnect the power supplies before connecting or changing the circuit. Do not connect the supplies if your partner is still working over the circuit.

3) Assume that the circuits are connected to the supplies unless proved otherwise.

4) Be sure that the measuring instruments are connected in correct places with sufficient ranges, and that there is not any ammeter in the voltmeter position and vice versa. Check over and over if the supply voltages are correct and DC measuring devices are connected with proper polarities.

5) Keep in mind that there may be charged capacitors in the circuit.

6) Some instruments need adequate cooling when they are in use. Do not obstruct the air flow by placing other equipment or papers on top of these units when they are operating.

7) Do not attempt to repair the instruments in the case you suspect of any fault. Report it to the assistants or technicians immediately.

8) Instruments and components must be neatly arranged on the table so that they can be checked easily.

9) Before making any attempt during the experiment, think and be sure of all its consequences. If you doubt, ask, if not carry on.

10) When the experiment is over, turn all the supplies and measuring devices off, disconnect the circuit, put all the instruments, components and wires away and clean your table.

USING LABORATORY INSTRUMENTS EFFECTIVELY

When measuring a physical quantity or using an instrument in an experiment, one should pay attention to the specifications of the instrument supplied by the manufacturer. These specifications may be shortly summarized under the following headings:

1. Connections:

Some instruments operate with an internal battery, some require the connection to 220 V mains supply and some do not need an internal or external supply connections.

The connection of an instrument to the circuit depends on the type of the instrument. For example, an ammeter must be connected in series with a component through which the current is to be measured. On the contrary, a voltmeter must be connected in parallel with the terminals across which the voltage is to be measured. An ohmmeter should never be connected across a resistor or any other circuit component which is excited by a current or voltage source.

2. Ranges:

Some instruments operate in AC and some in DC circuits.

Therefore, in such devices the selector switch should be positioned properly. Not only the type of the excitation circuit, but also the magnitude of the quantity to be measured or to be applied to the circuit is important. If different ranges are available on the instrument, the proper range should be selected before the power is fed into the circuit. Otherwise, the measuring instruments, the exciting sources and even the components appearing in the circuit can be damaged. For example, when applying a voltage or current, the range of voltage or current should be limited, otherwise some components such as resistors may get burn or some capacitors may blow up. A meter which is used out of its range may overdeflect and therefore its indicator (needle) may get twisted or the worst its coil can be damaged due to overheating.

3. Precautions:

Any instrument or device which is used out of its specified range is said to be overloaded. In most cases instruments are protected by fuses or cut-off knobs against wrong connection and overloading. However each protection has a nonzero response time so that the damage due to wrong connections and overloading may not be prevented. If a fuse burns out or a safety knob cuts off, the first thing to do is to check the connections and the range selected. After the error is removed, the fuse should be replaced or the push button cut-off knob is pressed. The general trend for the measurement devices is that the instrument should be positioned to its largest range. For the voltage and current sources,

however, the opposite is true, i. e., they must be positioned at their smallest ranges.

4. Accuracy:

None of the instruments, devices or components is perfect. A component may not have the exact component parameters specified by the manufacturer. For example, resistors are produced with typical 1%, 5%, 10% or 20% tolerances. An ammeter reading is reliable only with an accuracy such as 1% or 2% of its full scale deflection. However, more accurate instruments are available at higher prices. Manufacturers always give the accuracy of devices in catalogs or data sheets.

5. Scaling and Zero Adjustment:

Some measuring instruments such as voltmeters, ammeters and ohmmeters need to be adjusted before usage. For example, in order to adjust an ohmmeter for zero resistance, its measuring probes should be touched each other and the deflection should be adjusted to the zero reading by turning the proper knob or screw on the meter. Some devices such as the cathode ray oscilloscope have continuous adjustment knobs to scale the vertical and horizontal axes so that each division corresponds to some certain desired volts within some limits. There also exist voltage and time calibration pots on some oscilloscopes which must normally be turned in a certain direction (fully clockwise or counter-clockwise). In order to obtain results with higher accuracy from this type of instruments,

suitable calibrations must be performed before each experiment.

6. Frequency Response:

For instruments used under AC excitation, the lower and the upper limits of frequency always exist so that the instrument functions properly. For example, a typical avometer may detect voltages between 20 Hz and 20 KHz within a 3% accuracy which is usually smaller than the accuracy at 50 Hz for which it is normally designed. For this device, the accuracy decreases sharply for the frequency ranges out of the band 20 Hz-20 KHz, and the meter can not be used to measure AC voltages at all.

Similar frequency limitations always exist for power sources and circuit components as well. In fact, at very high frequencies all the lumped parameter circuit models break down and the classical circuit theory is not applicable at all.

7. Temperature Effects:

In general, the characteristics of any device change with temperature. For measuring instruments the variation due to temperature is expressed in "percent accuracy per degree centigrade Celsius (%/°C)". In a similar manner, for circuit components similar parameters are shown on the components. Every instrument, especially the digital ones, has the limits of the temperature range in which it functions correctly.

PRESENTATION OF LABORATORY NOTEBOOKS

Reports written in laboratory notebooks are intended to be a record of experiments carried out in the laboratory for the student. When examined, each report should give sufficient information about the experiment so that it can be repeated exactly at a later date without referring to the laboratory manual. The laboratory notebooks should be chosen and arranged according to the following regulations:

1) **Laboratory Notebook:** The laboratory notebook should be a 25-30 page, 21x30 cm with squared ruling or plane paper for one term experiments. Laboratory notebooks should be given to the assistants at the end of the semester (they will not be returned to the students).

2) **First page:** The first page contains a heading (i.e. EEE311 LAB or EEE312 LAB), student's name, class, number, group (name of the day on which the student attends to the laboratory) and the partner's name.

3) **Second page:** The second page contains an "Index of Experiments" that include name of the experiment and the page number at which the experiment starts. That means each page of the laboratory notebook must be numbered as 1, 2, 3, ... which is placed on the right hand side of the top of each page.

4) **Report:** A report for an experiment must contain the following entries:

a) **Title:** Experiment number, name of the experiment and the date at which the experiment is performed.

b) **Objective:** The purpose of the experiment.

c) **Preliminary:** All questions in the "Preliminary" section of the manual should be answered in detail.

The entries 1, 2 and 3 must be completed before coming to the laboratory.

d) **Experimental Procedure:** All the network diagrams should be drawn. The measurement readings recorded during the experiment must be included in a tabular form. The columns and rows of all tables must be clearly labeled with appropriate units included. The results presented in the graphical form should either be drawn on the page with ruler or on a proper graph paper that can later be stuck onto the notebook. The figures observed on the oscilloscope may be drawn directly to the notebook.

e) **Conclusions:** The conclusions must contain detailed answers to the questions given at the "Conclusions" part of experiment given in the manual. In addition, differences between the theoretical and practical results, if there exist other than the ones mentioned in questions and comments on these differences should be given in student's own words.

CHAPTER 2

INSTRUMENTS USED IN THE ELECTRONICS LABORATORY

AVOMETER (AVO)

AVOMETER MODEL 8 Mk 5

Avometer model 8 Mk 5 (simply will be referred to as AVO in the rest of the book) is a device which is used to measure current, voltage and resistance (Amperes, Volts, Ohms). The front view of AVO is shown in Fig. 2.1.

1. SPECIFICATIONS:

1.1. Table of ranges:

DC Voltage	*DC Current*	*AC Voltage*	*AC Current*
3000 V	10 A	3000 V	10 A
1000 V	1 A	1000 V	1 A
600 V	100 mA	600 V	100 mA
300 V	10 mA	300 V	10 mA
100 V	1 mA	100 V	
30 V	300 μA	30 V	
10 V	50 μA	10 V	
3 V		3 V	
100 mV*			

* on the 50 μA range

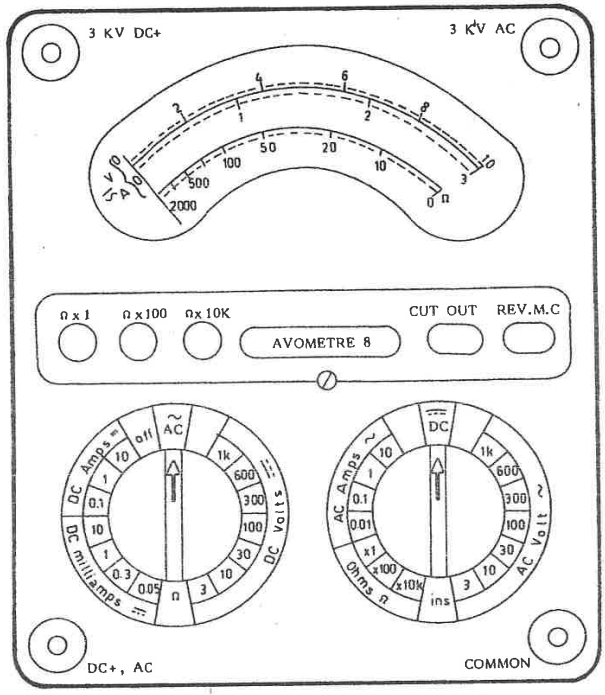


Fig. 2.1 AVO Model 8 Mk 5.

1.2. Resistance:

0-2000 Ω (20 Ω center scale), self-contained,

0-200 KΩ (2 KΩ center scale), self-contained,

0-20 MΩ (200 KΩ center scale), self-contained,

0-200 MΩ (2 MΩ center scale), with external voltage.

1.3. Accuracy:

DC Voltage & Current ranges	±1% of full scale deflection
AC Voltage & Current ranges (50 Hz)	±2% of full scale deflection

1.4. Sensitivity:

DC Voltage ranges	20000 Ω/V
AC Voltage ranges	2000 Ω/V (above 10 V)

1.5. Frequency response:

Variation from reading at 50 Hz, on AC voltage ranges up to 300 V and AC current ranges is not greater than ±3%, between 15 Hz and 15 KHz.

2. OPERATION:

2.1. General:

The meter is intended for use at horizontal position. If the indicator (pointer) is not on zero, it may be set by using the screw head on the panel. Do not attempt to set this zero position with the instrument set to OFF.

The leads fitted with clips should be connected to the lower pair of meter terminals except when measuring voltages over 1000 V.

When measuring current or voltage, ensure that the instrument is set to either AC or DC as appropriate and a suitable range before connecting up to the circuit under test. When in doubt, always switch to the highest range and work downwards, there is no necessity to disconnect the leads as the switch position is changed.

Do not switch off by rotating either of the knobs to a blank position.

2.2. Scaling:

The scale plate has three main sets of markings, each approximately 5 inches long, the innermost being for resistance measurement and is marked 0-200,000 Ω. The second and the third are for current and voltage (both AC and DC). The second one is marked 0-10 whilst the third scale calibrated 0-3 has 60 divisions.

2.3. Polarity reverse control:

If a polarity reversal is needed during DC voltage or current measurements, a polarity reverse press button (REV M.C.) is provided in order to simplify the matter of lead alteration. It should be noted that the polarity marked on the terminals is for normal use and does not apply when the red section of the REV M.C. button is extended.

2.4. Overload protection:

If an overload is applied to the meter, either forward or in reverse,

the CUT OUT knob springs from its normal position in the panel, thus breaking the main circuit and the red portion of the cut out knob will now be extended. This knob should only be depressed to render the instrument again ready for use. It is important to note that the cut out should never be reset when the instrument is connected to an external circuit, whilst the fault which has caused the overload should be rectified before the meter is reconnected.

Although the overload mechanism gives almost complete protection to the meter, it can not be guaranteed to completely fulfill its function in the very worst cases of misuse, such as the mains being connected across the meter when set to a current range. It should be noted that a mechanical shock to the instrument will sometimes trip the cut out mechanism. Additional protection is provided on resistance ranges by a fuse connected in the Ω×1 and Ω×100 ranges.

2.5. Current measurement:

To measure current, the instrument should be set to a suitable AC or DC range and then be connected in series with the circuit under test.

The voltage drop at the meter terminals is approximately 700 mV on the 10 A DC range, dropping to 100 mV on the 50 μA range. In the case of AC ranges it is less than 450 mV on all ranges. Standard meter leads have a resistance of 0.02 Ω per pair. Ensure that the circuit is 'dead' before breaking into it to make current measurements.

2.6. Voltage measurement:

When measuring voltage, it is necessary to set an appropriate AC or DC position and to connect the leads across the source of voltage to be measured. If the voltage is unknown, set the instrument to the highest range and decrease the ranges step by step until the most suitable range has been selected. If the measured voltage is greater than 1000 V, the positive lead should be transferred to the 3000 V position (that much voltage is not present in electronics lab).

On the DC ranges, the meter draws 50 μA at full scale deflection corresponding to 20 KΩ/V. In the case of AC ranges above 10 V, full scale deflection is obtained with a consumption of 0.5 mA (2 KΩ/V). The meter draws 1 mA and 10 mA on the 10 V and 3 V ranges respectively, at full scale deflection. The meter maintains a high degree of accuracy for audio frequency tests up to 15 KHz on ranges up to 300 V AC.

2.7. Resistance measurement:

There are three self-contained ranges covering from 1 Ω to 20 MΩ and provision is made for upward extension of these limits.

On resistance ranges, in addition to the normal instrument zero adjustment, the meter must have a resistance zero adjustment corresponding to the full scale deflection of the meter. Before carrying out tests for resistance, a check should be carried out to ensure that the meter actually indicates zero ohms irrespective of the condition of the

battery.

The accuracy, should be 3% of the reading about center scale, increasing up to about 10% of the indication around deflections corresponding to 10% and 90% of full scale deflection.

Resistance tests should never be carried out on components which are already carrying current.

On the three ranges which utilize the internal source of voltage, a positive potential appears at the negative terminal of the instrument when set for resistance tests. The resistance of some components varies according to the direction of the current through them and readings therefore, depend upon the direction in which the test voltage is applied quite apart from its magnitude. Such cases include electrolytic capacitors, diodes, rectifiers and transistors.

Before making the resistance tests the pointer should be adjusted to zero in the following sequence:

a) Set the left-hand switch at Ω.

b) Join leads together.

c) On the ohms ×1 range, adjust to zero by means of the knob marked Ω×1.

d) On the ohms ×100 range, adjust to zero by means of the knob marked Ω×100.

e) On the ohms ×10 K range, adjust to zero by means of the knob marked Ω×10 K.

The resistance is read directly on the Ω×1 range, but readings

should be multiplied by 100 and 10,000 on the Ω×100 and Ω×10K ranges, respectively.

If, on joining the leads together, it is impossible to obtain zero ohms setting, or if the pointer position will not remain constant, but falls steadily, the internal battery or cell concerned should be replaced. It is important that a discharged battery unit should not be left in the instrument, since it might cause damage to the meter. If it is impossible to obtain readings on the Ω×1 and Ω×100 ranges, the 1 A fuse located in the battery box should be checked.

DIGITAL MULTIMETER

(DMM)

FLUKE 8000A DIGITAL MULTIMETER

The model 8000A shown in Fig. 2.2 is a compact digital multimeter (DMM) featuring a 3½ digit display, push-button selection of range and function, auto polarity, self locating decimal point, self zeroing to eliminate offset uncertainties, and overload protection for all ranges.

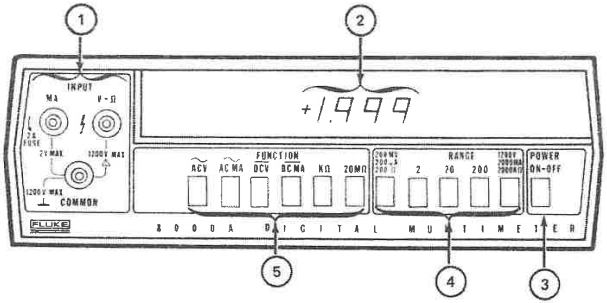


Fig. 2.2 Fluke 8000A digital multimeter (DMM) controls, indicators and connectors.
1. Input connetors, 2. Digital readout, 3. POWER switch
4. RANGE switches, 5. FUNCTION switches.

1. SPECIFICATIONS:

1.1. DC voltage:

Ranges: ±199.9mV, ±1.999V, ±19.99V, ±199.9V, ±1199V

Accuracy: ±(0.1% of reading + 1 digit)

Input impedance: 10 MΩ

Response time: 500ms

Max. input voltage: 1200Vdc or 1200Vrms (sinusoidal)

1.2. AC voltage:

Ranges: 199.9mV, 1.999V, 19.99V, 199.9V, 1199V

Accuracy: at 45Hz-10KHz ±(0.5% of reading + 2 digits),
at 10KHz-20KHz ±(1% of reading + 2 digits)

Input impedance: 10 MΩ//100pF

Response time: 3s, worst case

Max. input voltage: 1200Vrms (sinusoidal), not to exceed 10^7Volts-Hz product on 20, 200, 1200V ranges, 500Vrms (sinusoidal) on 200mV and 2V ranges.

1.3. Direct Current:

Ranges: ±199.9µA, ±1.999mA, ±19.99mA, ±199.9mA, ±1199mA

Accuracy: ±(0.3% of reading + 1 digit)

Response time: 500ms

Max. input: 2Arms (fuse protected).

1.4. Alternating Current:

Ranges: 199.9μA, 1.999mA, 19.99mA, 199.9mA, 1199mA

Accuracy: at 45Hz-10KHz ±(1.0% of reading + 2 digits) except 2000mA range,
at 45Hz-3KHz ±(1% of reading + 2 digits) on 2000mA.

Response time (within one range): 3s

Max. input: 2A rms (fuse protected).

1.5. Resistance:

Ranges: 199.9Ω, 1.999KΩ, 19.99KΩ, 199.9KΩ, 1999KΩ, 19.99MΩ

Accuracy: ±(0.2% of reading + 1 digit) on all ranges except 20MΩ,
±(0.5% of reading + 1 digit) on 20MΩ

Response time: 500ms on all ranges except 20MΩ, 4s on 20MΩ

Current through unknown: 1mA on 200Ω and 2KΩ
100μA on 20KΩ
1μA on 200KΩ and 2000KΩ
0.1μA on 20MΩ

Max. input voltage: 130Vrms on 200Ω and 2KΩ,
250Vrms on 20KΩ to 20MΩ

2. OPERATION:

Push-button controls allow the selection of five AC and DC voltage ranges, five AC and DC current ranges, and six resistance ranges. The measurement capabilities of the 8000A range from 100μV to 1199V

AC and DC, 100nA to 1.999 A AC and DC, and 100 mΩ to 19.99 MΩ.

The front panel readout features a 3½ digit display using light emitting diodes (LEDs). The display includes a self locating decimal point and a + or - polarity indicator. The full scale readout is 1999 for all ranges and functions except the 1200 V AC and DC range, which is 1199. A blinking full scale readout indicates that the 8000A is being operated in an overrange condition.

The front panel input connectors are banana type and provide separate connections for common, current, and volt-ohm inputs. Both the current and volt-ohm inputs are referenced to the common input. Common can operate at a potential of up to ±1200 Vp reference to earth ground.

The overload features of the 8000A include a fused current input and an overvoltage protected volt-ohm input. This protection applies for any function and range selected.

OSCILLOSCOPE (CRO)

TELEQUIPMENT TYPE D65

Cathode Ray Oscilloscope is also called shortly as CRO. The Telequipment D65 oscilloscope is shown in Fig. 2.3.

1. SPECIFICATIONS:

1.1. Vertical system:

Operating modes:

a) Channel 1

b) Channel 2 (normal or inverted)

c) Channels 1&2

Alternate

Chopped (at 150 KHz approx.)

Summed

d) X-Y

3 dB bandwidth:

DC coupled	DC-15 MHz
AC coupled	2 Hz-15 MHz
RisetimeX1	23ns nominal
X10 AC or DC coupled	10 MHz approx.
Max. amplitude	4 div (division) at 15 MHz

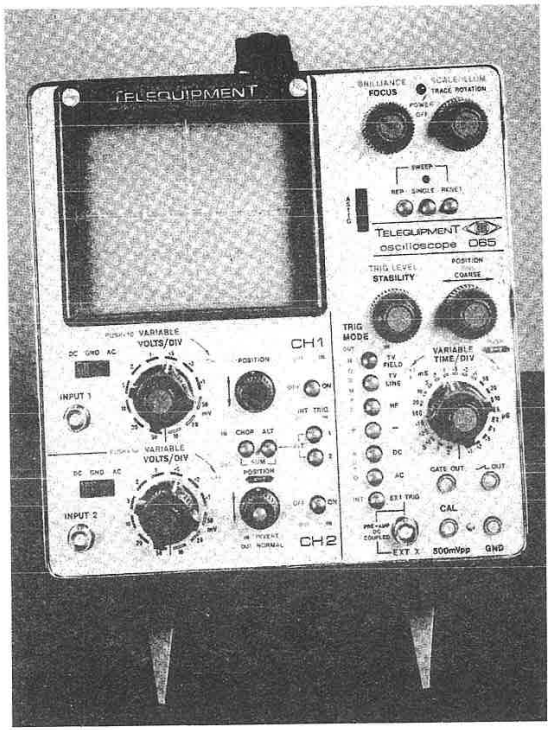


Fig. 2.3 Telequipment D65 oscilloscope.

X-Y: Via CH1 with CH2 input selected via timebase switch as horizontal amplifier.

Bandwidth (-3 dB)	DC-1 MHz
Phase error	Less than 1° at 25 KHz

Deflection factors:

Calibrated-accuracy ±5%	10 mV-50 V/div (12 ranges 1-2-5 steps)
Gain X10	1 mV-5 V/div
Uncalibrated-with variable	Complete cover between steps and to 125 V/div

Signal delay: 200 ns

Input impedance: 1 MΩ and 47 pF approx.

Max. input-DC, AC peak&Sum of: 400 V peak

1.2. Horizontal system:

Sweep generator:

Sweep rates

Calibrated (23 ranges 1-2-5 steps)

2 s-100 ns/div±5% without expansion;

±7% with X5 expansion, 40 ns/div fastest

Uncalibrated (with variable)

Complete cover between steps and to 5 s/div

Single shot (for displaying non-recurrnt signals)

With lock-out

External horizontal amplifier

3 dB bandwidth	DC-1 MHz
Risetime	350 ns nominal
Deflection factors	1 V/div approx 200 mV/div approx. (with X5 expansion)
Input impedance	100 KΩ and 30 pF approx.
Maximum input	400 V peak

1.3. Trigger:

Coupling: AC or DC

Source: CH1, CH2, alternate, and external

Internal:

Amplitude

Automatic

0.25 div (0.5 div at X10 gain) 40 Hz to 1 MHz

1 div at alternate

Trigger level

0.25 div (0.5 div at X10 gain) DC to 1 MHz,

rising to 0.5 div at 5 MHz

1 div at alternate

HF 1 div from 1 MHz to >25 MHz

External:

Amplitude	250 mV to ±15 V at above frequencies
Impedance	100 KΩ and 30 pF

1.4. Cathode ray tube (CRT):

Type:	Single-gun
Display area:	8 X 10 cm
Overall accelerating potential:	4 KV approximately.
External intensity modulation:	
Coupling	AC to grid
Amplitude, peak to peak	50 V max
	15 V for perceptible modulation at average brilliance
Time constant	10 ns

1.5. Outputs (front panel):

Calibrator, peak to peak:	500 mV square wave at supply frequency
Accuracy:	2%
Sweep sawtooth:	
Coupling	DC
Amplitude, peak	10 V approx.
Minimum load	47 KΩ
Gate out:	
Coupling	DC
Amplitude, peak	500 mV approx.

2. FUNCTION OF CONTROLS AND CONNECTORS:

2.1 CRT:

BRILLIANCE changes the intensity of the display.

FOCUS controls the definition (sharpness) of the display.

ASTIG (astigmatism) is used in conjunction with FOCUS for best overall definition

TRACE ROTATION rotates the traces about the horizontal axis of the CRT and is used to align the traces with the horizontal graticule divisions.

SCALE ILLUM (scale illumination) changes the intensity of the graticule illumination, as well as serving as the supply ON-OFF switch.

2.2. Horizontal display:

POSITION changes the location of the trace(s) on the horizontal axis, when not in the X-Y mode.

FINE acts as a more sensitive position control as well as the X5 horizontal gain switch. When pulled out in the X5 position, all sweep speed calibrations must be divided by 5. In the X-Y mode, FINE is inoperative, X5 gain is operative .

2.3. Sweep:

TIME/DIV (time/division) controls the speed of the main sweep. The sweep rates indicated are only valid if VARIABLE is fully clockwise and FINE position is pushed in for X1 gain. If FINE

position is pulled out and VARIABLE is at CAL, the calibration should be divided by a factor of 5 to ascertain the sweep speed.

VARIABLE enables speeds between that indicated by TIME/DIV and the next lower speed to be selected. The control also selects X-Y operation when the knob is pushed in.

LEVEL selects the point on the signal waveform at which the sweep starts. In the AUTO position, the trigger oscillates recurrently at a low repetition rate in the absence of a triggering signal; when a suitable signal is applied, the circuit is automatically triggered at the mean level of the input waveform.

STABILITY controls the sensitivity of the sweep generator, turned fully anti-clockwise prevents the sweep from running, while fully clockwise causes the sweep to free-run.

SINGLE SHOT assists in viewing or photographing a non-recurrent signal. If a recurrent signal is applied to the oscilloscope, in the SINGLE SHOT mode, the sweep will run once at each time RESET is pressed, when not in the X-Y mode.

2.4. Triggering mode:

TV F (TV field) and *TV L* (TV line) facilitates triggering from TV FIELD (frame) or line pulses; the level control may require adjustment for best results. Polarity relates to the sense of video modulation.

HF (high frequency) should be depressed for synchronization from high' frequency signals.

LEVEL can be adjusted for a locked sweep.

"±" provide triggering from the positive or negative-going slope of a waveform.

AUTO obtained by releasing DC and AC buttons.

INT (internal) and *EXT* (external) enable the sweep to be triggered either internally, from the vertical amplifier, or externally.

AC or *DC* relates to the coupling of the trigger circuit. For very low input frequency DC should be selected.

2.5. Vertical display CH1 & CH2:

OFF-ON release of these buttons switches off the channel concerned. If both channels are switched off, a straight line trace results which can not be shifted by the POSITION controls except when in the X-Y mode.

INT TRIG (internal triggering) selects triggering from either or both channels. When alternately triggering from both channels both INT TRIG buttons should be released; the display should be partially superimposed.

CHOP-ALT-SUM (chopped-alternate-summed) provides three display modes for the vertical channels.

In the CHOP mode, the channels are alternately switched on and off at a frequency of about 150 KHz; this mode is suitable at lower sweep speeds.

In the ALT mode, each channel is alternately displayed for

the duration of a sweep; the ALT mode is preferable at higher sweep speeds.

In the SUM mode, the display is the addition of the individual signals; CH1 POSITION is used to shift the trace, CH2 POSITION acts as a fine shift control. If INVERT is depressed, the resultant display is the difference between the two input signals.

POSITION displaces each trace in the vertical direction except when both channels are off.

In the X-Y mode, irrespective of button settings, CH1 provides a vertical shift and CH2 a horizontal shift.

INVERT-NORMAL determines whether the CH2 signal is displayed in the same polarity as the input signal, or inverted. The inverted setting is used to display the difference between two signals in the SUM mode.

VOLTS/DIV (volts/division) provides twelve steps of attenuation of each channel's input signal. Calibrated sensitivities are only valid when VARIABLE is fully clockwise The overall bandwidth is reduced to approximately 10 MHz.

VARIABLE enables all deflection sensitivities, between that selected by the VOLTS/DIV switch and the next below, to be covered. The control must be fully clockwise for a calibrated display; for X10 gain the knob should be pushed in.

DC-GND-AC (dc-ground-ac) selects the input signal coupling.

In the DC position the signal from the INPUT connector is coupled directly to attenuator.

In the AC position, a capacitor is inserted in series.

In the GND position, the input to the attenuator is grounded; this position enables the 0 V DC level of a trace to be ascertained.

3. OPERATION:

3.1. Pre-operational check:

Set the controls as follows before operate the device:

CRT:

Brilliance	Fully anti-clockwise
Focus	Central
Astig	Central
Trace rotation	As set
Scale illum	Fully anti-clockwise, POWER OFF.

Horizontal Display:

Position	Central
Fine	Central and pushed in
Stability	Fully clockwise
Time/div	5 ms
Variable	Fully clockwise
Level	Any position
Trig mode	All buttons out
Sweep	REP.

Vertical Display CH1 & CH2:

Off/on	ON
Int trig	1
Chop-alt-sum	CHOP
Position	Central
Invert-Normal	NORMAL
Volts/div	0.2 V
Variable	Fully clockwise
DC-GND-AC	GND

3.2. Operation steps:

a) Switch on with the SCALE ILLUM.

b) Allow a few minutes for warm-up, then adjust CRT and POSITION controls for a two-trace display. Adjust TRACE ROTATION if necessary to make the traces horizontal.

c) Apply the supply frequency squarewave from the CAL 500 mV peak to peak socket to both INPUT connectors via co-axial leads and switch DC-GND-AC to DC. Rotate STABILITY anti-clockwise to lock display.

d) If the supply frequency is 50 Hz, 2.5 cycles of the calibrator waveform will be displayed, each display being 2.5 div in amplitude.

SIGNAL GENERATOR (SG)

WAVETEK MODEL 180 SWEEP/FUNCTION GENERATOR

The Wavetek Model 180 Sweep/Function Generator, shown in Fig. 2.4, is a source of sine, triangle and square waveforms. Frequency of the waveforms is variable from 0.1 Hz to 2 MHz. The generator can repetitively sweep from one frequency to a higher frequency, with controllable rate and range of sweep. Amplitude of the waveforms is variable from 10 V peak-to-peak onto 50 Ω load down to 30 mVp-p. DC reference of the waveforms can be offset positively and negatively.

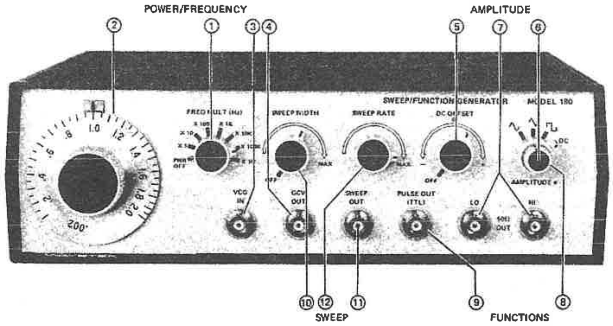


Fig. 2.4 Wavetek Model 180 Sweep/Function Generator controls and connectors.

The controls and connectors in Fig. 2.4 are:

1. Freq multiplier/power off
2. Frequency dial
3. VCG IN (Voltage controlled generator input) connector
4. GCV OUT (Generator controlled voltage) connector
5. DC offset
6. Amplitude
7. 50Ω OUT connector (HI:high, LO:low)
8. Waveform selection (sine, triangle, square and DC)
9. TTL (transistor-transistor logic) pulse OUT connector
10. Sweep width/off
11. Sweep OUT connector
12. Sweep rate

1. SPECIFICATIONS:

1.1. Output Signals:

Sine, triangle, square, TTL pulse, ramp and DC.

1.2. Control:

Generator operates in continuous and sweep modes. Frequency controlled manually or with external voltage.

1.3. Frequency range:

0.1 Hz to 2 MHz adjustable with the following ranges:

X1	0.1 Hz to 2 Hz
X10	0.1 Hz to 20 Hz
X100	0.2 Hz to 200 Hz
X1K	2 Hz to 2 kHz
X10K	20 Hz to 20 kHz
X100K	200 Hz to 200 kHz
X1M	2 kHz to 2 MHz

1.4. Main output:

Sine, triangle and square waveforms and DC are selectable. HI (0 dB) and LO (-20 dB) BNC outputs are available for simultaneous usage; outputs may be varied to HI (-30 dB) and LO (-50 dB) by amplitude control. HI output provides 20Vp-p maximum open circuit (10 Vp-p max. onto 50 Ω load). LO output provides 1 Vp-p max. onto 50 Ω load.

1.5. DC offset and DC output:

DC offset of waveforms and DC output are selectable and variable through HI and LO BNC outputs. HI output supplies ±10 V max. (±5 V onto 50 Ω load) as offset or Vdc output, LO output ±1 V max. into 50 Ω load as offset or Vdc output. Waveform offset is limited to ±10 Vp HI and ±1 Vp LO (both open circuit voltages).

1.6. Pulse output:

TTL pulse (50% duty cycle) at generator frequency can drive up

to 20 TTL loads.

1.7. GCV (Generator controlled voltage) output:

0 to 2 V (nominal, open circuit) proportional to frequency of main generator. Output impedance is 600 Ω.

1.8. VCG (Voltage controlled generator) input:

VCG voltage as well as control settings select generator frequency. Frequency may be DC-programmed or AC-modulated by an external 0 to 2 V signal. Input impedance is 2 KΩ. VCG input can change generator output 1000:1 on all ranges except X10 and X1 ranges. VCG input signal bandwidth is 100 KHz and slew rate is 0.1 V/μs.

1.9. Sweep output:

Ramp waveform output with 5 Vp into open circuit. Output impedance is 600 Ω.

1.10. Precision:

Horizontal:

Dial accuracy: ±3% of full scale for 0.1 Hz to 2 MHz.

Time symmetry: ±3% of full scale for 0.1 Hz to 2 MHz.

Vertical:

Amplitude change with frequency (Sine):

< ±0.1 dB on all ranges through X100K,

< ±0.5 dB on X1M range.

1.11. Waveform purity:

Sine distortion:

<0.5% on X100, X1K, X10K ranges (typically 0.2%).

<1.0% on X1, X10, X100K ranges (typically 0.5%).

All harmonics 30 dB down on X1M range.

Square wave rise and fall time:

<75ns.

Triangle linearity:

>99% to 200KHz.

2. OPERATION:

2.1. Continuous:

Operates as standard VCG. Frequency of main generator is determined by dial/range setting and VCG input voltage.

2.2. Sweep:

Main generator is frequency modulated by an internal sweep generator. When swept, main generator frequency rises from frequency set by the dial and range setting to a frequency set by sweep width control.

Sweep rate is continuously adjustable 30 ms to 20 s (nominal) by single turn control on front panel.

Sweep width is adjustable up to1:1000 on all ranges except X1 and X10 ranges.

DC POWER SUPPLY

COUTANT LQT 100

The LQT 100 power supply provide continuously variable, highly stable twin outputs which can operate in both constant voltage and constant current modes. These units, by front panel switch selection, can be operated in series or parallel as well as in the master/slave configuration. The front panel of LQT 100 power supply is shown in Fig. 2.5.

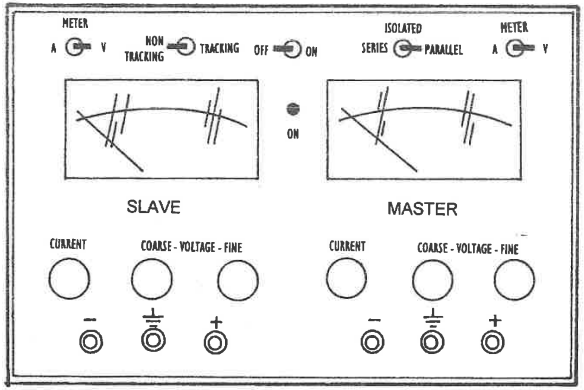


Fig. 2.5 Coutant LQT 100 DC power supply.

1. SPECIFICATIONS:

1.1. Constant voltage mode:

Line regulation : ± 0.01 + 1 mV for A ± 10% mains change

Load regulation : 0.03% + 3 mV zero to full load

Ripple voltage : 0.005% + 0.5 mV peak to peak.

1.2. Constant current mode:

Line regulation : ± 0.01 + 1 mA for A ± 10% mains change

Load regulation : 0.03% + 3 mA zero to full load

Ripple voltage : 0.01% + 1 mA peak to peak.

1.3. Available outputs:

Output voltage	*Output current*
0 to 30 V twice	0 to 1 A twice
0 to 60 V	0 to 1 A
0 to 30 V	0 to 2 A
Variable -30 to +30 V tracked about zero.	Variable -1 A to +1 A tracked about zero.

1.4 Controls:

On-Off controls the mains input supply to the unit and is indicated when ON by a light.

V-A switches enable either voltage (V) or current (A) to be monitored on the appropriate meter.

Tracking/Nontracking enables the unit to work in the master/slave mode of operation.

Series/Isolated/Parallel enables the two outputs to be connected in series or parallel.

Voltage: Two single turn potentiometer per output provide coarse and fine control to set the output voltage level.

Current: One single turn potentiometer per output sets the output current level.

2. OPERATION:

2.1. Two independent outputs:

a) Select "isolated" position on the series/parallel switch.

b) Select "nontracking" position on the tracking/non-tracking switch.

2.1.1. Constant voltage mode:

a) Select "V" position on V/A switches.

b) Turn all voltage controls to minimum (fully anti-clockwise) and the current control to maximum (fully clockwise).

c) Connect the load/loads to the output terminals and adjust the voltage until the required level is indicated on the meter. The unit will remain in constant voltage mode unless the load resistance is so reduced that the current demand exceeds the level set by the current control (i.e. capacity of the unit if fully clockwise), the output will then enter into the constant current mode and the voltage will fall to maintain a constant

current output.

2.1.2. Constant current mode:

a) Select "A" position on V/A switches.

b) Turn all voltage controls to maximum (fully clockwise) and the current control to minimum (fully anti-clockwise).

c) Connect the load/loads to the output terminals and adjust the current controls until the required current level is indicated on the meter. The unit will remain in constant current mode until the load resistance is so increased that the current demand less than the level set by the current control, the unit will then change to the constant voltage output.

2.2. Master/Slave operation:

a) Select "tracking" position.

b) Select "series" position.

c) Connect loads to output terminals as follows:

2.2.1. Constant voltage mode:

a) Select "V" position on V/A switches.

b) Turn all voltage controls on master unit to minimum (fully anti-clockwise) and the current control on master unit to maximum (fully clockwise).

c) With the loads connected to the output terminals, adjust the master unit voltage until the required level is indicated on the master unit

meter. The -O/P will remain at the corresponding level (with respect to zero) as the +O/P. The unit will remain in constant voltage unless the load resistance is so reduced that the current demand exceeds the level set by the current control (i.e. capacity of the unit if fully clockwise), the unit will then enter the constant current mode and the voltage will fall to maintain a constant current output.

2.2.2. Constant current mode:

a) Select "A" position on V/A switches.

b) Turn master unit current control to minimum (fully anti-clockwise) and the voltage controls to maximum (fully clockwise).

c) With the loads connected to the output terminals, adjust the master unit current control until the required level is indicated on the master unit meter. The -O/P will remain at the corresponding level (with respect to zero) as the +O/P. The unit will remain in constant current unless the load resistance is so increased that the current demand is less than the level set by the current control, the unit will then change to constant voltage operation.

2.3. Series operation:

a) Select "series" position.

b) Select "tracking" position.

c) Connect load to the extreme outside terminals.

2.3.1. Constant voltage mode:

a) Select "V" position on V/A switches.

b) Turn all voltage controls on master unit to minimum (fully anti-clockwise) and the current control on master unit to maximum (fully clockwise).

c) With the loads connected to the output terminals, adjust the master unit voltage until half the required level is indicated on the master unit meter. The voltage level will always be twice that shown on the master unit meter. The unit will remain in constant voltage unless the load resistance is so reduced that the current demand exceeds the level set by the current control (i.e. capacity of the unit if fully clockwise), the unit will then enter the constant current mode and the voltage will fall to maintain a constant current output.

2.3.2. Constant current mode:

a) Select "A" position on V/A switches.

b) Turn master unit current control to minimum (fully anti-clockwise) and the voltage controls to maximum (fully clockwise).

c) With the loads connected to the output terminals, adjust the master unit current control until the required level is indicated on the master unit meter. The unit will remain in constant current unless the load resistance is so increased that the current demand is less than the level set by the current control, the unit will then change to constant voltage operation.

2.4. Parallel operation:

a) Select "parallel" position.

b) Select "non-tracking" position.

c) Connect load to one set of terminals (i.e. the master unit O/P terminals or to slave unit terminals).

2.4.1. Constant voltage mode:

a) Select "V" position on V/A switches.

b) Turn voltage controls (both master and slave units) to minimum (fully anti-clockwise) and the current controls to maximum (fully clockwise).

c) With the load connected to the output terminals, adjust the both unit voltage controls until the required level is indicated on both meter. The unit will remain in constant voltage unless the load resistance is so reduced that the current demand exceeds twice the level set by the current control (i.e. twice the capacity of the unit if fully clockwise), the unit will then enter the constant current mode and the voltage will fall to maintain a constant current output.

2.4.2. Constant current mode:

a) Select "A" position on V/A switches.

b) Turn both current controls to minimum (fully anti-clockwise) and the voltage controls to maximum (fully clockwise).

c) With the load connected to the output terminals, adjust the urrent controls until the required level is indicated on both meter. It is mportant that both unit currents are set to the same level (as far as is ossible). The unit will remain in constant current unless the load esistance is so increased that the current demand is less than the level set y the current control, the unit will then change to constant voltage peration.

HIGH VOLTAGE POWER SUPPLY (HVPS)

HEATH MODEL SP-17A

Heath SP-17A Regulated HV (high voltage) power supply, shown in Fig. 2.6, is a compact, convenient source of variable regulated high voltage, variable bias voltage, and filament voltage for laboratories and workshops. Separate panel meters are provided for accurate monitoring of the DC output current and voltage. All output binding ports are insulated from the chassis to allow the high (B+) and bias (C-) voltages to be used as either negative or positive voltage sources.

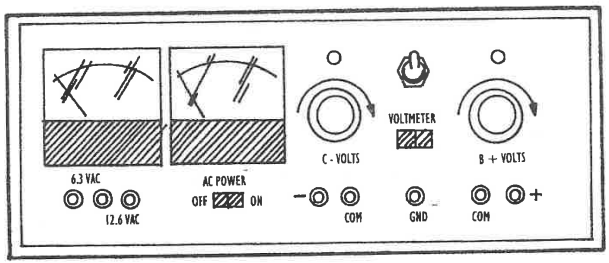


Fig. 2.6 Heath SP-17A high voltage power supply.

1. SPECIFICATIONS:

1.1. B+ Volts Output:

Voltage	0 to 400 Vdc, regulated
Current	0 to 100 mA continuous, 125 mA intermittent
Regulation	Output variation less than 1% from no load to full load for output of 100 to 400 Vdc. Output variation is less than ±1% for a ±10% variation of the 115 V or 230 V AC input source.
Ripple	<10 mVrms ripple, jitter and noise
Output impedance	<10 Ω from DC to 1 MHz.

1.2. C- and Filament Volts Output:

C- volts	0 to -100 Vdc at 1 mA
Filament voltage	6.3 V AC at 4 A, or 12.6 V AC at 2 A (Note: these outputs may be used at the same time provided that the total power does not exceed 25 VA).

1.3. General:

Output binding posts	Common and + (B+ voltage)
	Common and - (C- voltage)
	6.3 V AC at 4 A
	12.6 V AC at 2 A
Front panel controls	AC power switch
	DC ON-Standby switch
	Voltmeter switch
	C- volts control
	B+ volts control
Circuit board controls	Zero voltage adjust
	400 V adjust

1.4. Meters:

Volts, Dual scale	0 to 400 and 0 to 150 V DC (accuracy:±3% of full scale)
Milliamperes	0 to 150 mA (accuracy:±2% of full scale)

2. OPERATION:

Separate transformers are used for filament and high voltage supplies so the filament circuit may be left on while switching off the high voltage circuit. This eliminates repeated tube warmup time.

A meter switch permits you to monitor either the high voltage or the bias voltage on the front panel voltmeter. The special taper C-VOLTS control provides a finer adjustment of low values of bias voltage. Built-in circuit protection prevents damage if the bias voltage output circuit should accidentally be short circuited or overloaded, and the input circuit of the Regulated HVPS is fused with additional protection against overload conditions or short circuits.

BREADBOARD

The breadboard present on each set of Electronics Laboratory is shown in Fig. 2.7. It is composed of a type SK-10 breadboard socket and 2+3=5 binding posts placed on an aluminum case.

1. BINDING POSTS:

Binding posts are connected to the breadboard by the external wiring structure denoted by the curved lines in Fig. 2.7.

It is preferable to use the binding posts in the following way:

Binding post #1	$+V_s$ (signal generator)
Binding post #2	$-V_s$ (signal generator)
Binding post #3	+V (DC power supply)
Binding post #4	0V Ground (DC power supply)
Binding post #5	-V (DC power supply)

2. BREADBOARD LAYOUT:

Type SK-10 breadboard is composed of a total of 840 tie-points. The solid lines between the tie points show the internal wiring structure of the breadboard. According to this structure:

a) Binding posts 3, 4 and 5 are connected to the horizontally shorted lines. If the external connection wires exist in the middle

(denoted by bridge wires in the figure), the whole horizontal line connected to 3, 4 and 5 will be at the same potential (shorted).

b) Regions A and B, each has 64 vertical lines composed of 5 tie-points. Every vertical line of these 5 tie-points are connected to each other internally. The channel between regions A and B is open circuit. If an IC is to be connected to the breadboard, it must be placed across this channel (e.g. pins at the top connected to the bottom of region A and the ones at the bottom connected to the top of region B).

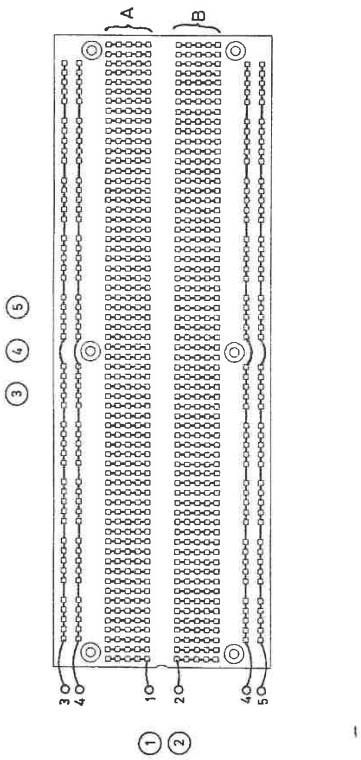


Fig. 2.7 Breadboard layout.

CHAPTER 3

EXPERIMENTS

EXPERIMENT

1

INTRODUCTION TO THE INSTRUMENTS USED IN ELECTRONICS LABORATORY

OBJECTIVE:

Introduction to the equipment and components used in Electronics Laboratory, obtaining i-v characteristics and frequency response of some devices.

THEORY:

Refer to the specifications of the instruments given in Chapter 2 and the experimental procedure below.

PRELIMINARY:

Revise your knowledge about the usage of equipment used in Electronics Laboratory reading Chapter 2 "Specifications of the Instruments used in Electronics Laboratory".

EXPERIMENTAL PROCEDURE:

■ **Important:** You'd better measure voltage with the digital multimeter (DMM) and current with AVO since these devices produce more accurate readings than those on the DC power supply.

E1. Limiting the short-circuit current of the DC power supply:

When a short-circuit occurs in an experimental set-up, the equipment and components can be damaged by the high current passing through them. In order to avoid this problem, the short-circuit current of DC power supply must be limited before each experiment. Follow the given steps for short-circuit current limitation (you can do it for master or slave, or for both if you need to use both of them):

a) Turn current control to minimum (fully counter-clockwise).

b) Connect a cable across the output terminals (+ and - are shorted).

c) Select 'A' position of the V/A switch on the power supply. Increase the current slowly until the required short-circuit current is reached (200 mA in this experiment).

d) Select 'V' position of the V/A switch on the power supply and turn the voltage until the desired voltage is adjusted (7 V in this experiment).

E2. i-v characteristics of the DC power supply:

Use the digital multimeter (DMM) and AVO to measure the

voltage and current, respectively.

a) Keeping the voltage and current settings as in E1, connect the resistance decade box across the DC power supply as shown in Fig. 3.1.

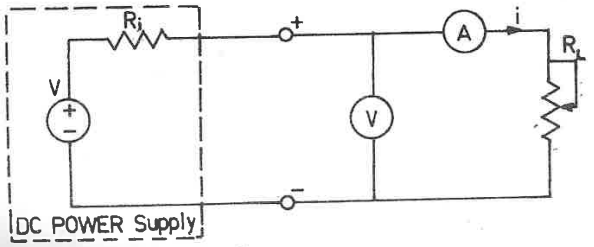


Fig. 3.1 Circuit to obtain i-v characteristics of DC power supply.

b) Change the value of R_L through the steps given in the following table. Measure and record the voltage and current at each step.

R_L (Ω)	∞	90K	10K	1K	100	50	40	30	20	10	0
i (mA)											
V (V)											

c) Draw the i-v curve using the data obtained in part b.

d) Making use of Fig. 3.1, determine the input resistance (R_i) of

the power supply at short-circuit (i.e. R_L=0) condition.

E3. Voltage and frequency calibration of the oscilloscope:

Normally, the voltage and frequency calibration controls on the oscilloscope (red buttons on Volt/Div and Time/Div switches) must be turned fully clockwise.

If you measure a previously known voltage with the CRO but read a different value, you must make the voltage calibration of that terminal. The same applies to the frequency calibration.

In order to make voltage or frequency calibration, the calibration output present on the CRO can be used. This terminal gives 500 mV_{p-p} square wave at 50 Hz.

Follow the procedure to make the voltage (or the frequency) calibration:

a) Connect the calibration output of the CRO to the inputs 1 and 2 of the CRO.

b) Measure the amplitude (frequency) of the signal and compare with the original calibration signal amplitude (frequency). If they are different, adjust the voltage (frequency) calibration control until the original value is reached.

E4. Use of signal generator (SG):

a) At sinusoidal waveform position of the signal generator and a frequency of 50 Hz, measure the maximum and minimum voltage output

(peak) of your signal generator for both high output (HI) and low output (LO) cases. Record these data in the following table.

SG output	*Max. voltage (V)*	*Min. voltage (V)*
HI output		
LO output		

Signals having both AC and DC parts can be obtained from the signal generator by following the steps given below:

a) Get (2sinωt) V at 50 Hz from the signal generator.

b) While keeping (2sinωt) V unchanged, adjust (3+2sinωt) V and (-3+2sinωt) V from the signal generator using the DC off-set button. Observe the waveforms on the CRO and draw them.

c) Keeping (2sinωt) V unchanged, increase the off-set voltage in both (+) and (-) directions and determine the off-set voltages which correspond to the maximum undistorted output for each case. Record these values in the following table.

Max. off-set in (+) direction	Volts
Max. off-set in (-) direction	Volts

E5. Obtaining the frequency response of DMM, AVO and CRO:

DMM, AVO and CRO can all measure voltages precisely at low frequencies, especially around 50 Hz. At higher frequencies, however,

the values read from these devices start to deflect from the real values, because some electronic components in these devices can not respond to high frequencies. Above some definite frequency, known as the **cutoff frequency** of the device, they can not measure the quantities correctly.

In order to obtain the frequency response of any device, its output is recorded at different frequencies. Follow the procedure to get the frequency response of DMM, AVO and CRO:

a) Adjust the signal generator output to (2sinωt) V at 50 Hz and measure it with the CRO. Connect this output to the measurement devices (i.e. DMM, AVO and CRO) at the same time.

b) Change the frequency through the steps given in the following table and record the voltages read from each device at each step.

c) Draw the frequency response of each device (i.e. voltage versus frequency).

f (Hz)	10	100	1 K	10	100 K	150 K	200 K	300 K	500 K	1 M
DMM										
AVO (V)										
CRO (V)										

CONCLUSIONS:

C1. What is the importance of the value of the load resistance connected to the DC power supply? Will there be any problem if the load resistance is too low?

C2. Which of the measurement devices, DMM, AVO or CRO, is more precise at high frequencies (f>100 KHz)?

EQUIPMENT LIST:

Resistance decade box

Standard set equipment (given in Chapter 2).

EXPERIMENT

2

DIODE CHARACTERISTICS, MODELING AND DIODE CIRCUITS

OBJECTIVE:

Introduction to diodes, diode characteristics, modeling circuits and other diode circuits.

THEORY:

T1. Diode test:

A quick way of determining whether a diode is defective or not is to use an ohmmeter. If the internal battery of the ohmmeter forward biases the diode, a large current will pass through it and a low resistance is read. On the other hand, reversing the diode should show a high resistance. For defective diodes, the ratio of the reverse to forward resistance approaches unity.

Note that, DMM has a forward internal battery (red jack is +), while AVO has a reverse internal battery (red jack is -). DMM is always

preferable to AVO in diode testing.

T2. Obtaining the i-v characteristics of a device or circuit:

To obtain i-v characteristics of any device or circuit with CRO, we can make use of Fig. 3.2. In this circuit, D denotes the device or circuit whose i-v characteristics will be obtained. Since the voltage versus current curve is to be obtained, both + and - voltages at different magnitudes must be applied to the circuit. This can be done using a sine wave, since it covers + and - values.

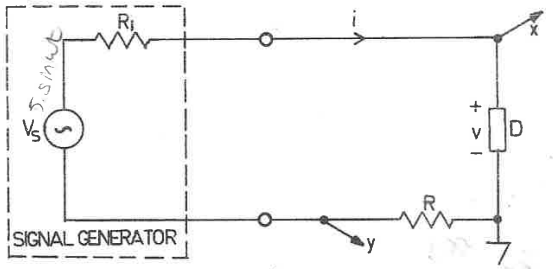


Fig. 3.2 Circuit for obtaining the i-v characteristics of any device or circuit.

Since CRO can not measure current directly, we can read current as follows: A series resistance (R) is connected to the circuit and the voltage drop on it (V_R) is measured. Then dividing the voltage by the

resistance gives the current ($i=V_R/R$).

R and V_S values should be chosen carefully for the determination of the correct characteristics. They must be chosen according to the device or circuit whose characteristics is to be obtained. For instance, if I_{max} of a rectifier diode is 1 A, we can not take $V_S=(10\sin\omega t)$ V and R=5 Ω, since $(V_S-V_\gamma)/R>1$ A which may damage the diode. A forward voltage drop of 0.7 V is enough to operate the diode, but $V_S>>(0.7\sin\omega t)$ V must be applied to the circuit in order to obtain the whole curve (i.e. the saturation and cut-off regions in addition to the ON region). As another example, consider a 6.2 V zener diode. If $V_S<(6.2\sin\omega t)$ V is applied to the circuit, the diode can not reach the zener action and the correct characteristics can not be obtained. For this diode, at least 10 V (peak) will be needed. However, the voltage should not be increased to a value which can cause reverse breakdown.

Note that, y input of the CRO in Fig. 3.2 is allocated for current measurement, while x input measures voltage. In order to see i-v characteristics on the CRO, push xy mode button placed on the Time/Div switch.

PRELIMINARY:

P1. Design a circuit which results in the i-v characteristics given in Fig. 3.3 (i.e. calculate the voltage and resistor values).

P2. Calculate and draw the transfer characteristics of the diode clipper given in Fig. 3.5.

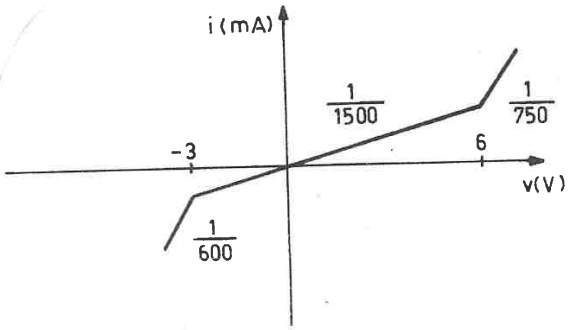


Fig. 3.3 i-v characteristics of an unknown circuit (for P1).

EXPERIMENTAL PROCEDURE:

E1. Diode test:

a) Test your diodes with both DMM and AVO.

E2. Diode i-v characteristics:

The specifications of different types of diodes used in this experiment are given in Table 3.1. These specifications are given for the user to operate the device in proper conditions. While obtaining the i-v characteristics, V_S and R values, in Fig. 3.2, for each diode must be chosen taking these data into account. It must be noted that the specified maximum voltage and current values should not be exceeded at the

maximum output of the signal generator (SG). For instance,

- for the rectifier diode, V_S and R must be chosen such that $i_{max}<$ 1 A,
- for the LED, V_S must be limited to 5 V peak,
- for the zener, $V_S>6.2$ V peak.

a) Construct the circuit of Fig. 3.2 with $V_S=(5\sin\omega t)$ V and R=100 Ω to the observe the i-v characteristics of the rectifier diode. Observe and draw the characteristic curve.

Code	*Type and material*	*Specifications*
1N4001	rectifier, Si	I_{max}=1 A, $V_{r(max)}$<50 V
MV5353	LED, GaP	I_f=35 mA, $V_{r(max)}$<5 V
BZX8506V	zener, Si	V_z=6.2 V, $P_{D\,max}$=200 mW

Table 3.1 Specifications of three different types of diodes.

b) Repeat part a for the LED, with $V_S=(3\sin\omega t)$ V and R=100 Ω. Observe the light emission from the LED.

c) Repeat part a for the zener diode, with $V_S=(10\sin\omega t)$ V and R=100 Ω.

d) Determine r_f, V_γ , V_z and r_z for each diode (if exist) using characteristic curves and fill in the following table.

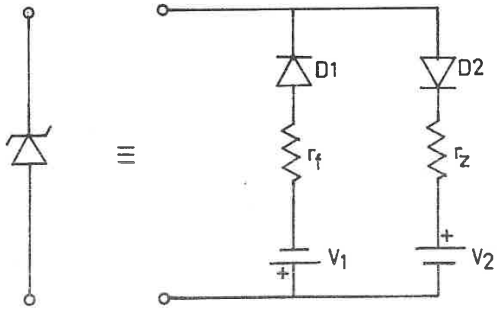


Fig. 3.4 A zener diode and its diode model circuit equivalent.

a) Choose the model circuit parameters with the help of the data obtained in E2d (for the zener diode).

b) Obtain and draw the i-v curve of this zener model using Fig. 3.2 (replace D with the zener diode whose anode is connected to the ground reference).

c) Compare the curve obtained in part b with the zener characteristics obtained in E2c.

E5. Diode circuits:

A) Diode clipper (limiter):

a) Construct the clipper circuit given in Fig. 3.5.

b) Obtain and draw the transfer characteristics (V_o-V_i) of this

Diode type and code	$r_f(\Omega)$	V_γ (V)	V_z (V)	$r_z(\Omega)$
rectifier (1N4001)				
LED (MV5353)				
zener (BZX8506V2)				

E3. Modeling:

a) Construct the model circuit designed in P1. Use the circuit given in Fig. 3.2 to obtain the i-v characteristics of this model circuit. Replace D with your circuit and take V_S=(10sinωt) V.

b) Observe and draw the i-v curve indicating the break voltages and currents. Compare this curve with the one given in Fig. 3.2 and explain the differences between them if there exist.

E4. Simulating the zener diode characteristics with a diode model circuit:

A model circuit for a piecewise linearized zener diode characteristics is shown in Fig. 3.4. The zener diode parameters $V_{\gamma z}$, V_z, r_f, and r_z are related to the model circuit parameters by the relations

$$V_{\gamma z} = V_1 + V_{\gamma 1}$$

$$V_z = V_2 + V_{\gamma 2}$$

circuit for sine, triangular and bipolar square wave inputs (V_i=10 V peak, at 100 Hz).

c) For the sine wave input, compare the slopes and break points with the theoretical calculations carried out in P2.

d) Decrease V_1 and V_2 to zero and see the "squaring" property of the circuit for the applied sine wave and draw it.

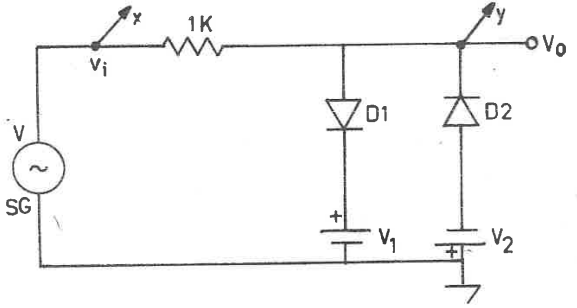


Fig. 3.5 Diode clipper (V_1=3 V, V_2=6 V).

B) Diode clamper:

a) Construct the clamper circuit in Fig. 3.6.

b) Apply sine, triangular and bipolar square waves to the circuit and draw v_o for each (V_i=10 V peak, at 100 Hz, V_B=5 V).

c) With R_L=∞ and R_L=100 KΩ, change V_B arbitrarily and observe that the input signal is clamped to V_B+V_γ at the output.

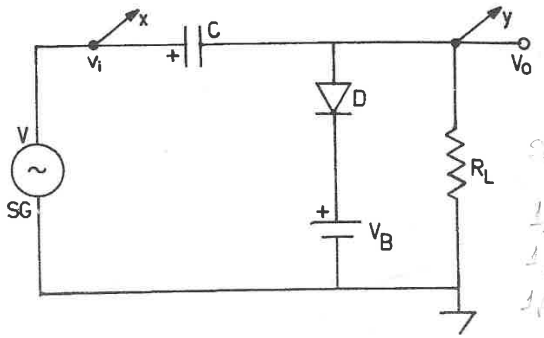


Fig. 3.6 Diode Clamper (C=100μF).

CONCLUSIONS:

C1. Could you observe the difference between ignoring V_γ and taking it into account while dealing with diode circuits?

C2. What is the function of the capacitor used in the diode clamper circuit?

C3. Compare the results of the diode clipper (E5A) and clamper (E5B) circuits for the sine, triangular and bipolar square wave inputs.

EQUIPMENT LIST:

Resistors (100, 150, 500, 1 K, 2*1.5 K, 10 K, 100 K)Ω

Capacitor (100) μF

Rectifier diodes (2*1N4001)

LED(MV5353)

Zener diode [BZX8506V2 (6.2 V)]

Standard set equipment.

EXPERIMENT

3

DIODE RECTIFIER CHARACTERISTICS

OBJECTIVE:

To demonstrate the application of diodes in rectifier circuits.

THEORY:

DC and AC voltages and currents serve the power requirements of the wide variety of electronic devices. Because it is more efficient and economical to transmit, AC power is generally distributed by the power networks. This necessitates the rectification (changing) of AC into DC voltages and currents.

Direct current is the current which flows in only one direction. The diode with unidirectional current characteristics is the best choice to accomplish rectification, since it permits current to flow in only one direction. Silicon, germanium, selenium and copper oxide rectifiers are solid-state devices which serve as power rectifiers. However, the silicon types are the most widely used ones in electronics today. A wide range

of silicon rectifiers exist which can deliver load currents from 200 mA to 1000 A, whose PIV (peak inverse voltage) ratings vary from 100 to more than 1000 V.

There are mainly two types of rectifier circuit configurations, half-wave and full-wave rectifiers.

In a **half-wave rectifier** as shown in Fig. 3.7, only the positive alternation cycles pass through the diode and result in a voltage drop on the load resistance. During the negative alternation, there is no current in the circuit, because the anode is negative with respect to the cathode, i.e. the diode is reverse biased.

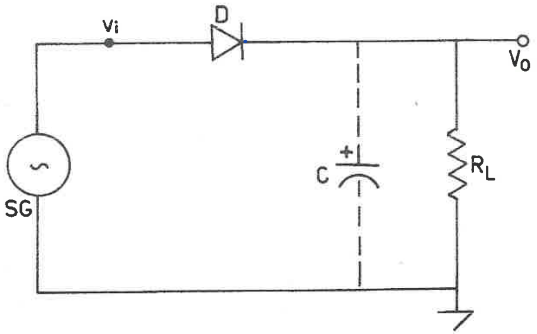


Fig. 3.7 Half-wave rectifier.

Full-wave rectifiers can be constructed in two different ways. One of them is the **bridge rectifier** shown in Fig. 3.8 that utilizes 4 diodes

and a two terminal transformer (secondary of the transformer can be considered as the SG in Fig. 3.8). On the other hand, the **center-tapped rectifier** configuration given in Fig. 3.9 consists of 2 diodes and a center-tapped transformer. The secondary side of the center-tapped transformer has three terminals with the voltage from each end to the center is exactly corresponds to the half of the total voltage across the secondary (i.e. $V_1=V_2$). Operating principles of the bridge and center-tapped full-wave rectifiers are different than each other.

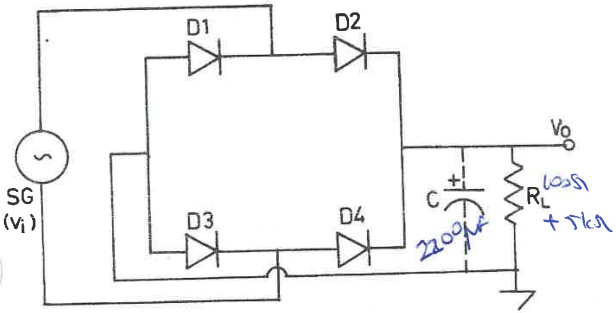


Fig. 3.8 Full-wave bridge rectifier.

PRELIMINARY:

P1. Rederive the equation

$$V_{dc} = V_m - \frac{T\, I_{dc}}{4\, C}$$

P3. Calculate the peak-to-peak ripple voltage $V_{r(p-p)}$ for a half-wave rectifier with R_L=2.2 KΩ and

a) C=10 μF, b) C=470 μF.

EXPERIMENTAL PROCEDURE:

- Check your diodes with DMM.
- Use the 6.3 V_{rms} output of HVPS (50 Hz) as signal generator output throughout the procedure.

E1. Half-wave rectifier:

a) Set up the circuit shown in Fig. 3.7 (R_L=2.2 K).

b) Sketch the input and output voltages on the same scale. Note a voltage difference of V_γ between the input and output.

c) Connect a 10 μF capacitor across R_L (dashed lines in the figure) and observe the effect of charge storage property of the capacitor on the load voltage. Measure $V_{r(p-p)}$ with the CRO (ac mode). Sketch the input and output voltages on the same scale.

d) Repeat part c using a 470 μF capacitor.

E2. Full-wave bridge rectifier:

- **Important:** Do not try to measure the input and output of full-wave rectifier circuit (with CRO) at the same time, since they do not have a common ground.

a) Set up the circuit shown in Fig. 3.8 (R_L=2.2 K).

for a full-wave bridge rectifier circuit with an output capacitor C. Assume negligible diode forward resistances and large C.

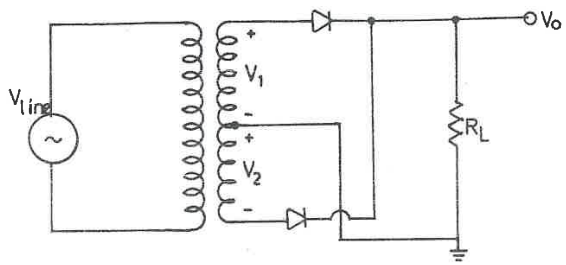


Fig. 3.9 Full-wave center-tapped rectifier.

P2. Explain the differences between the bridge and center-tapped rectifier circuits. Answer the following question:

Assume a 10:1 center-tapped transformer is used as step down transformer in a rectifier circuit. The output of this transformer is connected to a rectifier with load R_L. Assume that the primary side of the transformer is connected to 220 V_{rms} and V_γ=0.7 V for all diodes. Calculate and draw the output waveform if

a) the rectifier is bridge type (center terminal of the secondary side of the transformer is not connected),

b) rectifier is center-tapped type.

b) Sketch the input and output voltages on the same scale. Note a voltage difference of $2V_\gamma$ between the input and output.

c) Connect a 10 μF capacitor across R_L and observe the effect of charge storage property of the capacitor on the load voltage. Measure $V_{r(p\text{-}p)}$ with the CRO (ac mode). Sketch the input and output voltages on the same scale.

d) Repeat part c using 470 μF and 2200 μF capacitors, respectively.

e) Connect a 100 Ω resistor and a 5 KΩ pot in series instead of R_L in Fig. 3.8 (C is still 2200 μF).

f) Change R_L (pot) from 5 KΩ to zero with 500 Ω steps. At each step, measure

DC output voltage V_{dc} (with DMM)

DC output current I_{dc} (with AVO)

Peak-to-peak ripple voltage $V_{r(p\text{-}p)}$ (with CRO-ac mode).

Plot V_{dc}-I_{dc} and $V_{r(p\text{-}p)}$-I_{dc} curves using the measured data.

E3. Voltage doubler:

a) Set up the circuit in Fig. 3.10 using R_L=2.2 K, C_1=C_2=470 μF.

b) Plot the input voltage and the output voltage on R_L on the same time (ωt) scale.

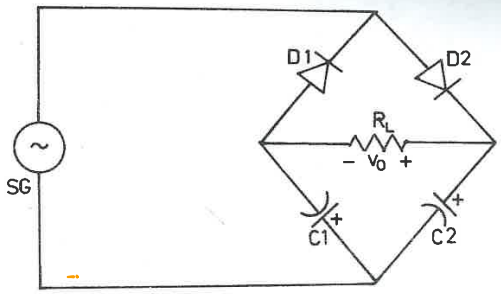


Fig. 3.10 Voltage doubler.

CONCLUSIONS:

C1. Compare the results obtained in the preliminary and experiment.

C2. What is the function of the capacitor at the output of a rectifier? Which of the following, a low capacitance or a high capacitance, results in a better rectification? Why?

EQUIPMENT LIST:

Resistors (100, 2.2 K)Ω

Potentiometer (5 K)Ω

Capacitors (10, 2*470, 2200)μF

Rectifier diodes (4*1N4001)

Standard set equipment.

EXPERIMENT

4

ZENER DIODES

OBJECTIVE:

To construct a zener voltage regulator and experimentally determine the range over which the zener maintains a constant output voltage.

THEORY:

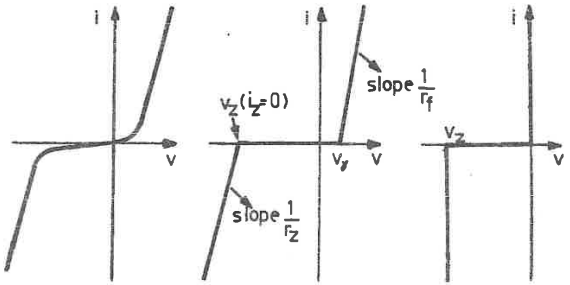
T1. Zener diode i-v characteristics:

When reverse biased, a pn junction exhibits a constant voltage region. This constant voltage is called as the **zener voltage** or the **breakdown voltage** and it is due to the avalanche effect or zener effect. In ordinary pn junctions, the avalanche effect is dominant and the breakdown voltage is in the order of a few hundred volts. However, for the zener diodes in which the zener effect is dominant, the zener voltage is in the order of several volts.

A typical zener diode i-v characteristics curve is given in Fig.3.11. As it is obvious from the characteristics, the zener diode must be reverse biased in order to be operated in the zener region. If a zener

diode is forward biased, it acts as a normal (rectifier) diode.

For design purposes, the true i-v characteristics must be used. However, for simplification in calculations, the use of the piecewise linearized model is preferred in this experiment. This model consists of forward and reverse resistances (r_f and r_z) and voltages (V_γ and $V_z[i_z=0]$). Using this model, $V_z[i_z=0]$ and r_z values are enough for calculations.



a) b) c)

Fig. 3.11 Zener diode i-v characteristics: a) true, b) piecewise linearized, c) ideal.

Zener diodes are used as voltage regulators and as voltage reference standards.

T2. Zener voltage regulators:

Fig. 3.12 shows the circuit of a zener diode used as a shunt

regulator (the zener diode is parallel with the load resistor R_L). The purpose of using the zener diode is to maintain a constant voltage across the load, within required limits, either as the output of the DC supply changes or as the load resistance, and hence the load current.

A) Changing the load resistance (i.e. output current):

As a numerical example, assume V=16 V, R=50 Ω, and the load current i_L changes between 10 mA and 50 mA.

The load line equation is,

$$V_z = V - R(i_z + i_L)$$

or

$$V_z + R\,i_z = V - R\,i_L$$

for the given parameters,

$$V_z + 50\,i_z = 15.5 \qquad \text{(for } i_L\text{=10 mA)}$$

$$V_z + 50\,i_z = 13.5 \qquad \text{(for } i_L\text{=50 mA)}$$

If the zener diode characteristics is given, it is possible to obtain a graphical solution for the maximum and minimum voltages, and the voltage swing at the output by following the procedure given below:

i) Using the load line equation given above, load lines obtained for each load current are drawn on the zener curve.

ii) From the intersection of these load lines and the zener characteristic line, the maximum and minimum output voltages, and the maximum output voltage swing can be found graphically.

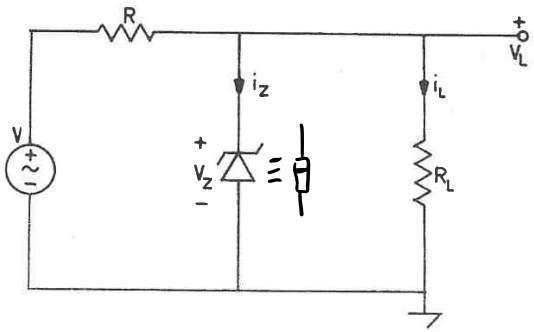


Fig. 3.12 Zener diode used as a shunt voltage regulator.

B) Variable input voltage:

As a numerical example, assume V=(16+1cosωt) V, R=50 Ω, and the load current i_L=100 mA.

In this case, the load line equation becomes,

$$V_z + 50\,i_z = (11 + 1\cos\omega t)$$

From this equation we obtain two load line equations for the maximum and minimum values of cosωt (i.e. 1 and -1). These are,

$$V_z + 50\,i_z = 12 \qquad \text{(for V=17 V)}$$

$$V_z + 50\,i_z = 10 \qquad \text{(for V=15 V)}$$

respectively.

For the graphical solution, the procedure given in T2A must be repeated.

PRELIMINARY:

P1. Assume a piecewise linearized zener diode model with r_z=5 Ω and $V_z[i_z=0]$=9 V. Find the maximum and minimum output voltages and the maximum swing at the output for the case given in T2A. Follow the procedure given below:

a) Draw the piecewise linearized zener diode model to scale.

b) Using the load line equations, draw the load lines obtained for each load current (to the same scale as in a).

c) From the intersection of these load lines and the characteristic line, find the maximum and minimum output voltages and the maximum output voltage swing.

HINT: While drawing the load line, first assume V_z=0 and find i_z, then assume i_z=0 and find V_z.

P2. Repeat P1 for the case in T2B using the same zener diode given in P1.

EXPERIMENTAL PROCEDURE:

E1. Set up the voltage regulator circuit given in Fig.3.13 (C=220 μF, R=100 Ω, R_L=470 Ω).

a) Draw the voltage waveforms at points A and B (seen on CRO).

b) Remove the zener diode and repeat part a.

c) Replace the zener diode, remove the capacitor and repeat part a.

E2. Replace R_L with 2200 Ω and repeat E1a.

E3. Replace the capacitor with 2200 μF and repeat E1a and E1b.

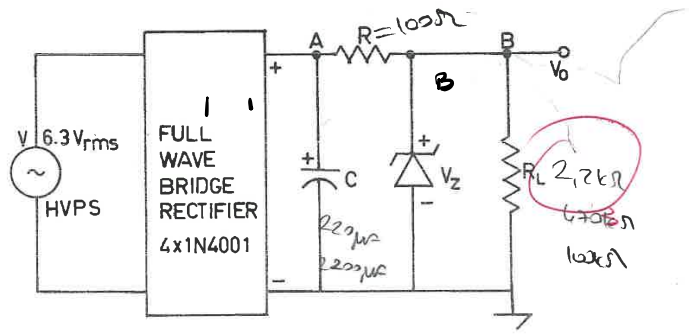


Fig. 3.13 Experimental zener diode voltage regulator.

CONCLUSIONS:

C1. Compare the results obtained in the preliminary and experiment.

C2. Calculate the ripple factors at point B, for procedures E1 and E2.

C3. Is zener diode useful for regulated power supply applications? Why?

EQUIPMENT LIST:

Resistors (100, 470, 2.2K)Ω

Capacitors (220 ,2200)μF

Rectifier diodes (4*1N4001)

Zener diode [BZX8506V2 (6.2 V)]

Standard set equipment.

EXPERIMENT

5

OPTOELECTRONIC DEVICES

OBJECTIVE:

To get data for LEDs, to display numbers with a seven-segment display and to transfer a signal through an optocoupler.

THEORY:

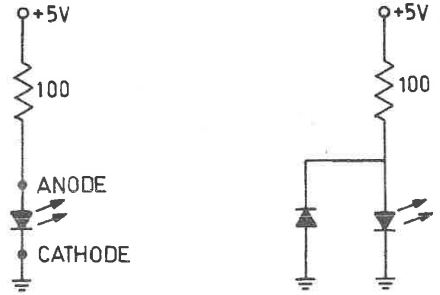
Optoelectronics is the technology that combines optics and electronics. This field includes light-emitting diodes (LEDs), LED displays, optocouplers, laser diodes, etc.

T1. LEDs:

The light-emitting diode (LED) is a solid-state light source having the following advantages over the conventional light sources: Low voltage, long life (more than 20 years) and fast on-off switching (ns range).

In a forward-biased rectifier diode, free electrons and holes recombine at the junction. When a free electron falls into a hole it drops

from a higher energy level to a lower one. As the electron falls, it radiates energy in the form of heat and light. The schematic symbol for a LED is shown in Fig.3.14a.



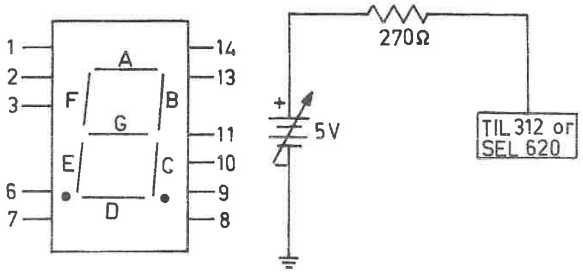
a) b)

Fig. 3.14 a) Forward-biased LED, b) protecting the LED against reverse bias.

LEDs have a typical voltage drop from 1.5 V to 2.5 V for currents between 10 and 50 mA. The exact voltage drop depends on the color, tolerance and other factors. LEDs have low reverse voltage ratings. For instance, the TIL221 has a maximum reverse voltage rating of 3 V. This means that, accidently applying a reverse voltage greater than 3 V may destroy the LED. One way to protect a led against an excess reverse voltage is connecting a rectifier diode in parallel as shown in Fig. 3.14b. The rectifier diode barrier voltage of 0.7 V prevents the reverse voltage

on the LED from exceeding that value.

T2. LED arrays:



a) b)

Fig. 3.15 Seven-segment display SEL620. a) Pinout, b) circuit schematic.

A LED array is a group of LEDs that display numbers, letters or other symbols. The most common LED array is the seven-segment display shown in Fig. 3.15a (pinout for SEL620 is also included). The display contains seven rectangular LEDs. Each LED is called a segment, because it forms a part of the character being displayed. Fig. 3.15b shows the circuit schematic in which a positive voltage drives all anodes. By grounding one or more cathodes through a current-limiting resistor, we can display any digit as well as some letters of the alphabet. Some

displays have positive common point as in this case and some have negative common.

T3. Photodiodes:

A reverse biased diode has a small current flowing through because of its minority carriers. The number of these carriers depends on the temperature and the light striking the junction. When a diode is in a glass package, the incoming light changes the amount of the reverse current because of the photoelectric effect (light changing an electrical quantity).

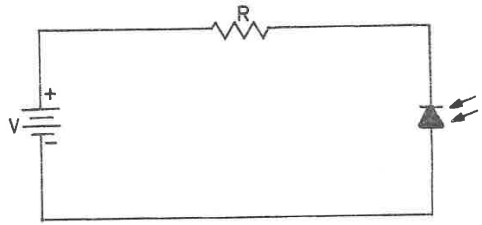


Fig. 3.16 Photodiode is reverse biased.

A photodiode is optimized for its sensitivity to light. In this diode, a glass window lets the light pass through the package to the junction. The incoming light produces free electrons and holes. In other words, the light increases the number of minority carriers. The stronger the light, the more minority carriers produced.

Fig. 3.16 shows the schematic symbol of a photodiode. The inward arrows represent the incoming light. Also notice that the photodiode is reverse-biased. In this way, as the light become more intense, the reverse current increases. The reverse current is small, typically in tens of microamperes.

The photodiode is one example of a photodetector, a device that can convert incoming light into electrical quantity. Other examples of photodetectors are photoresistors, phototransistors, etc.

T4. Optocouplers:

An optocoupler combines a LED and a photodetector in a single package. Fig. 3.17 shows an optocoupler. The LED supply forces current through the LED. The light from the LED hits the photodiode and sets up a reverse current through the resistor R_2. The voltage across the photodiode is given by

$$V_o = V_{SS} - IR_2$$

This output voltage depends on how large the reverse current is. If we change the supply voltage of the LED, the amount of light given by the LED changes and this causes the photodiode current to change. If the LED current has an AC variation, V_o will also have an AC variation. The most important advantage of an optocoupler is that, the input and the output circuits are completely isolated and the light provides the only contact between the circuits (because of this feature, optocoupler is also

known as optoisolator). This feature is a very useful fact in some applications that requires isolation of input and output circuits.

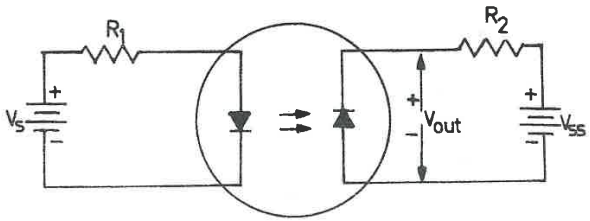


Fig. 3.17 An optocoupler circuit (arrows show light transfer).

EXPERIMENTAL PROCEDURE:

- Check your diodes with DMM.

E1. Data for a LED:

a) Examine the LED. There are three ways to determine the anode and cathode of a LED: You can determine anode and cathode with DMM or, as in many LEDs, the cathode lead (leg) is slightly shorter than the anode lead. Another way is to look inside the glass package: The anode part inside the package is small compared to cathode.

b) Connect the circuit of Fig. 3.18 using the red LED. The AVO is connected as an ammeter that measures the current through and the DMM measures the voltage across the LED. The rectifier diode 1N4001

protects the LED against accidently applying a high reverse voltage.

c) Adjust the source voltage V_S to pass 10 mA through the LED. Record the voltage across the LED. Increase the LED current with 10 mA steps, up to 40 mA, and record the LED voltage at each step. Plot the i-v characteristics of the LED using the measured data.

d) Repeat the above procedure (a to c) for the green LED.

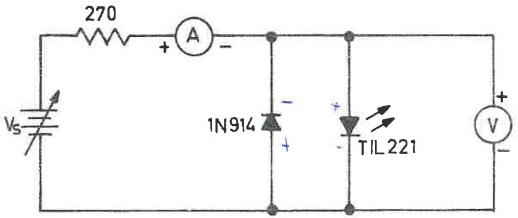


Fig. 3.18 Circuit for LED data.

E2. Using seven-segment display:

a) Fig. 3.15a shows the pinout for the seven-segment display. It includes a right decimal point (RDP). Connect the circuit of Fig. 3.15b.

b) By grounding different pins, display the digits 0 to 9, and the decimal point (RDP). While displaying each digit, record the grounded pins.

E3. The transfer graph of an optocoupler:

a) Connect the optocoupler circuit given in Fig. 3.19. Adjust the source voltage V_S from 0 to 14 V, with 2 V steps. Measure and record the corresponding output voltages at each step.

b) Draw the transfer graph (V_o versus V_S) of the optocoupler using the data obtained in part a.

c) Apply $V_S = (8+2\sin\omega t)$ V, from SG, to the circuit. Measure V_o and V_S (separately) with CRO and draw them on the same scale. Take the data obtained in part a into account (the maximum output corresponds to the minimum input).

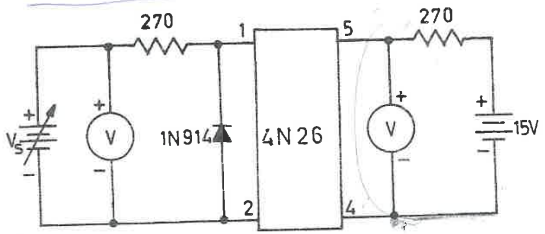


Fig. 3.19 An optocoupler application circuit.

CONCLUSIONS:

C1. Why are the photodiodes reverse biased?

C2. What is the main advantage of using optocouplers?

C3. Compare the voltage drops on the red and green LEDs recorded when 20 mA current passing through them. Explain the reasons for the differences if there exist.

EQUIPMENT LIST:

Resistors (2x270)Ω

Rectifier diode (1N4001)

LEDs [TIL221 (red) and TIL222 (green)]

Display (SEL620 or TIL312, seven-segment)

Optocoupler (4N26 or 4N27)

Standard set equipment.

EXPERIMENT

6

BIPOLAR JUNCTION TRANSISTOR (BJT) FAMILIARIZATION AND CHARACTERISTICS

OBJECTIVE:

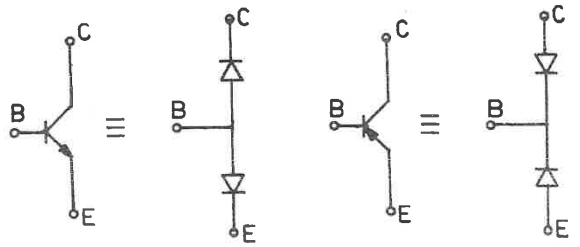
To become familiar with the Bipolar Junction Transistors (BJT) and to investigate the output (collector) and input (base) characteristics of BJTs.

THEORY:

T1. Introduction to BJT:

BJT is a three-terminal device comprised of the emitter (E), the collector (C) and the base (B) leads (regions). There are two types of BJTs according to the doping of these three regions. The **npn** BJT, shown in Fig. 3.20a, have n-type emitter and collector, and p-type base. The opposite doping types are true for the **pnp** BJT shown in Fig. 3.20b. For the purposes of biasing and test, a BJT can be modeled by two diodes

as shown in Fig. 3.20. Arrow directions show the actual emitter current (I_E) direction for both types. Collector current I_C of a BJT is controlled by the base current I_B.



a) b)

Fig. 3.20 Symbol and diode equivalent of BJT a) npn type, b) pnp type.

T2. BJT operating regions:

There are three BJT operating regions as shown in Table 1. V_γ voltage declared in this table is dependent on the material of the BJT. If BJT is made up of Silicone (Si), V_γ can be taken as 0.7 V, if it is Germanium (Ge), V_γ=0.3 V, unless otherwise stated. $V_{CE(sat)}$ is also material dependent and is about 0.2 V for Si, 0.1 V for Ge BJTs. $V_{CE(sat)}$ can be taken as zero in calculations, for simplicity, if not given. Be careful that the polarities of voltages are given for npn transistor in Table 3.2. For pnp transistors these polarities must be reversed.

1. Active region: A BJT operating in active region can be used as an amplifier. For this region, the emitter-base junction must be forward biased while the collector-base junction must be reverse biased. In this case, a base-emitter voltage drop of $V_{BE}=V\gamma$ is present and both the majority and minority carriers flow through the collector.

Region	***Biasing of B-E, B-C***	V_{BE} I_B	V_{CE} I_C
active	B-E forward B-C reverse	$\approx V\gamma$=0.7 V (Si), =0.3 V (Ge) >0	>0 βI_B+I_{CEO}
cutoff	both reverse	$V_{BE}\leq 0$ 0	>0 0
saturation	both forward	$\approx V\gamma$=0.7 V (Si), =0.3 V (Ge) $>I_{C(sat)}/\beta$	$\approx V_{CE(sat)}$=0.2 V(Si), =0.1V(Ge) $I_{C(sat)}$*

Table 3.2 BJT operating regions (for npn type). *$I_{C(sat)}$ is determined by external circuit elements.

In active region, the collector current can be written as,

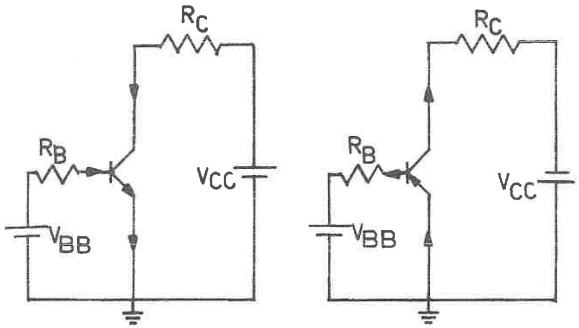
$$I_C = I_{C\ majority} + I_{C\ minority}$$

$$= \alpha I_E + I_{CO}$$

$$= \beta I_B + (\beta + 1) I_{CO}$$

$$I_C = \beta I_B + I_{CEO}$$

where, $I_E=I_C+I_B$ and $\beta=\alpha/(1-\alpha)$, I_{CO} represents the open-emitter collector-to-base (for npn BJT) leakage current (also denoted as I_{CBO} in some books), I_{CEO} represents the open base leakage current passing through collector to emitter (for npn BJT). Actual current flow directions of I_{CO} and I_{CEO} for pnp transistors are the opposite of those for npn transistor. The active region biasing for both npn and pnp BJTs and actual current flow directions are shown in Fig. 3.21.



a) b)

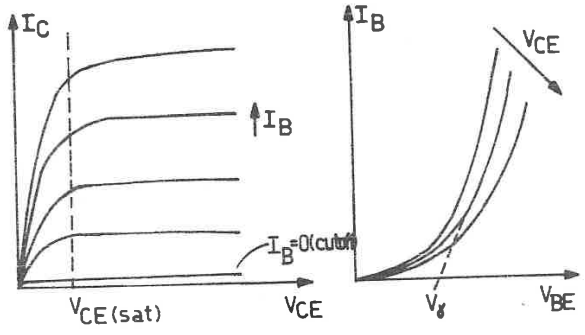
Fig. 3.21 Basic BJT amplifier biasing for a) npn, b) pnp types.

Typical npn BJT collector (output) and base (input) characteristics are given in Fig. 3.22. Note from Fig. 3.22a that, as the I_B is increased, I_C increases as well. If V_{CE} is near zero ($V_{CE(sat)}$ in fact) transistor saturates. The saturation current $I_{C(sat)}$, determined by the

external circuit elements, can be written for the circuit in Fig. 3.21a as,

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \approx \frac{V_{CC}}{R_C}$$

On the other hand, if I_B is decreased to zero, the transistor is cut off and no I_C flows anymore. The base characteristics shown in Fig. 3.22b is similar to the characteristics of a forward biased rectifier diode.

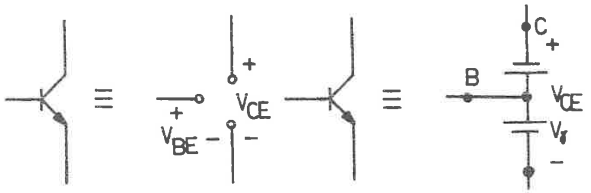


a) b)

Fig. 3.22 npn BJT a) collector and b) base characteristics.

2. Cutoff region: Since both the emitter-base and collector-base junctions are reverse biased, no current flows through the junctions and BJT junctions can be considered as open circuit. The DC equivalent circuit of a BJT at cutoff is given in Fig. 3.23a.

3. Saturation region: When both emitter-base and collector-base junctions are forward biased, transistor saturates and a saturation current flows through the collector. Since both junctions are forward biased, V_γ voltage drop is seen across each diode as shown in Fig. 3.23b. $V_{CE(sat)}$ is the difference between the V_γ values of heavily doped emitter-base and lightly doped collector-base junctions. If $V_{CE(sat)}$ is neglected, collector emitter junction can be considered as short circuit. Be careful that $I_C \neq \beta I_B$ in saturation.



a) b)

Fig. 3.23 BJT DC equivalent circuits at: a) cut-off and b) saturation.

PRELIMINARY:

P1. Starting with $I_E=I_C+I_B$, $I_C=\alpha I_E+I_{CO}$ show that $I_C=\beta I_B+I_{CEO}$ where $\beta=\alpha/(1-\alpha)$ and $I_{CEO}=(\beta+1)I_{CO}$.

P2. If $V_\gamma=0.7$ V, $\beta=100$ for the transistor in Fig. 3.26, and $V_{CC}=12$ V, $V_i=4$ Vp-p square wave at 100 Hz, draw V_i and V_o on the same scale.

P3. Use the values given in P2 and $V_{CC}=(8+4\sin\omega t)$ V at 10 Hz instead of $V_{CC}=12$ V, draw V_i and V_o on the same scale for a period of $\sin\omega t$.

EXPERIMENTAL PROCEDURE:

■ Test your BJT using DMM in KΩ range.

E1. Collector (output) characteristics:

a) Connect the circuit of Fig. 3.24 and observe the collector (output) characteristics of an npn transistor (i.e. I_C-V_{CE} curve) on the CRO.

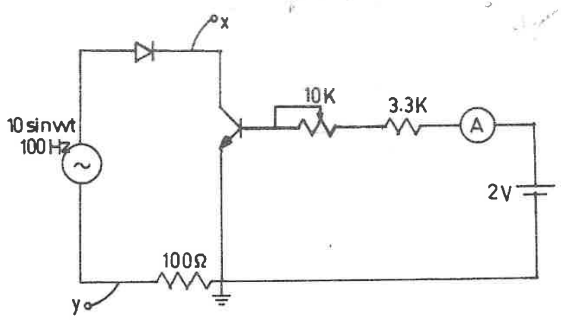


Fig. 3.24 Circuit to obtain collector (output) characteristics of an npn BJT.

b) By changing the pot, adjust I_B from 0 to 400 μA with 100 μA steps, observe and draw I_C-V_{CE} curve at each step. Compare the characteristics with the one given in Fig. 3.22a.

E2. Base (input) characteristics:

a) Connect the circuit of Fig. 3.25 and observe the base (input) characteristics of an npn transistor (i.e. I_B-V_{BE} curve) on the CRO.

b) By changing the pot, adjust V_{CE} from 0 to $V_{CE(max)}$ with 4 equal steps, observe and draw I_B-V_{BE} curve at each step. Compare the characteristics with the one given in Fig. 3.22b.

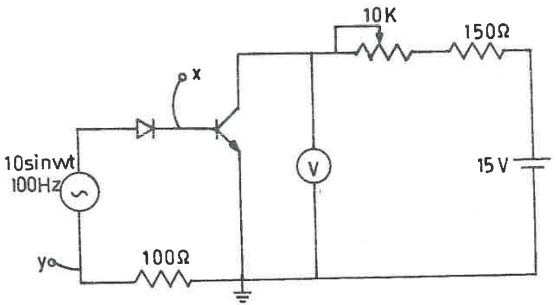


Fig. 3.25 Circuit to obtain base (input) characteristics of an npn BJT.

E3. BJT analog switch:

Knowing that I_C=0 at cutoff and I_C= $I_{C(sat)}$ at saturation, a BJT

can be used as an analog switch as in Fig. 3.26. At cutoff, V_o=V_{CE}=V_{CC} since I_C=0, and at saturation V_o=$V_{CE(sat)}$=0.2 V (or ≈0).

a) Connect the circuit of Fig. 3.26 and adjust V_i=4 V_{p-p} square wave at 100 Hz.

b) Observe and draw the waveforms on both x (V_i) and y (V_o) inputs of CRO. Compare the result with the one you calculated in P2.

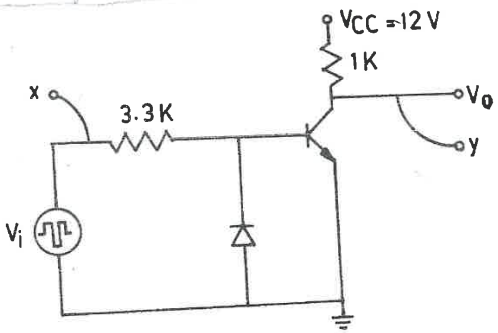
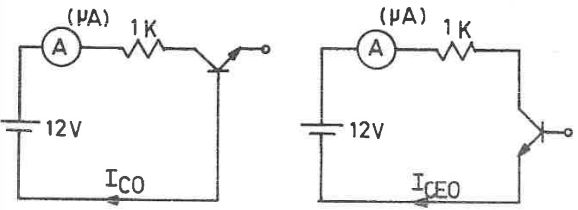


Fig. 3.26 BJT analog switch.

E4. Measurement of I_{CO} and I_{CEO}:

a) Connect the circuit of Fig. 3.27a and measure I_{CO} with AVO (in μA scale), and with CRO (measure the voltage on the resistor and divide by the resistance).

b) Connect the circuit of Fig. 3.27b and measure I_{CEO}, using both methods explained in E4a.



a) b)

Fig. 3.27 Circuits for the measurement of a) I_{CO} and b) I_{CEO}.

ONCLUSIONS:

1. What is the function of the diodes in Fig. 3.24 to 3.26?
2. Draw Fig. 3.24 and 3.25 for the pnp transistor.

QUIPMENT LIST:

sistors (100, 150, 1 K, 3.3 K)Ω
tentiometer (10 K)Ω
ctifier diode (1N4001)
T (BC237-npn)
andard set equipment.

EXPERIMENT

7

BJT BIASING AND THERMAL CHARACTERISTICS

OBJECTIVE:

Introduction to basic BJT biasing schemes and the thermal properties of BJTs.

THEORY:

In order to be used as an amplifier, the base-emitter junction of a BJT must be forward- and the collector-emitter junction must be reverse biased. For an amplifier, it is desirable that it operates at a constant **quiescent point** (also called **operating point**), or shortly **Q-point**. However, because of the temperature dependence of some BJT parameters, the operating point may remarkably change from the design values if the temperature is changed. Another problem is the large β range for a given transistor (for instance, β is between 200 and 400). This stems from the uncertainties during manufacturing process.

T1. Temperature dependent BJT parameters:

There are mainly three temperature dependent parameters as:

i) V_{BE} (base-to-emitter voltage drop) decreases as the temperature is increased,

ii) I_{CO} (collector-base junction leakage current) increases as the temperature is increased,

iii) β (current amplification factor) almost increases linearly with temperature.

If the temperature rises from T_1 to T_2, and BJT parameters at T_1 are known, these parameters at T_2 can be calculated using the relations given below:

$$V_{BE2} = V_{BE1} + (-2\ mV/°C)\ \Delta T$$

$$I_{CO2} = I_{CO1}\ 2^{(\Delta T/10)}$$

where $\Delta T = T_2 - T_1$. Unfortunately, there is no well-known relation explaining the temperature dependency of β.

The change in the collector current due to the change in V_{BE}, I_{CO} and β can be calculated by taking the effect of one parameter into account while the others are assumed to be constant. For this purpose, stability factors (S factors) of the circuit with respect to each parameter must be calculated. These factors are defined as

$$S_V = \frac{\Delta I_{CQ}}{\Delta V_{BE}} \approx \frac{\partial I_{CQ}}{\partial V_{BE}}$$

$$S_I = \frac{\Delta I_{CQ}}{\Delta I_{Co}} \approx \frac{\partial I_{CQ}}{\partial I_{Co}}$$

$$S_\beta = \frac{\Delta I_{CQ}}{\Delta \beta} \approx \frac{\partial I_{CQ}}{\partial \beta}$$

Right hand-side of these equations are reasonable if the changes in the independent variables are assumed to be small. In these equations,

$$\Delta V_{BE} = V_{BE2} - V_{BE1}$$

$$\Delta I_{Co} = I_{Co2} - I_{Co1}$$

$$\Delta \beta = \beta_2 - \beta_1$$

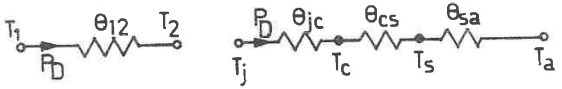
where subscripts 1 and 2 denote the parameter values at temperature T_1 and T_2, respectively. The total change in I_C current due to the change in these parameters can be written as,

$$\Delta I_{CQ} \approx S_V\ \Delta V_{BE} + S_I\ \Delta I_{Co} + S_\beta\ \Delta \beta$$

As it is clear from this relation, the smaller the S, the higher the stability. It is also desirable that the changes in the parameters are small.

T2. Heat flow, thermal resistance and heat sink:

In order to reduce the temperature changes that cause Q-point instabilities, medium power and high power transistors are made of metal cases which increase heat convection to ambient. Moreover, if the use of metal case can not solve the problem alone, some **heat sinks** are attached to the metal case to make better cooling. It is also common to use **cooling fans** to overcome the heating problems in very high power systems. In this way, the variations in I_{CQ} due to the variations in V_{BE}, I_{CO} and β can be kept at minimum. For a better understanding on transistor cooling, let us introduce some heat transfer concept and make a connection with the electrical systems (i.e. electron transfer).



a) b)

Fig. 3.28 a) A simple thermal system, b) transistor thermal circuit equivalent.

The thermal resistance between two points of a conductive system, as shown in Fig. 3.28a, can be written as,

$$\Theta_{12} = \frac{T_1 - T_2}{P_D}$$

where, Θ_{12} is the thermal resistance between the points 1 and 2 (similar to electrical resistance), T_1 and T_2 are the temperatures at the points 1 and 2 (similar to voltage), and P_D is the heat or power input (similar to current). Using the simple Ohm's Law approach, thermal circuits can easily be analyzed.

For a transistor with heat sink, the complete transistor thermal circuit can be shown as in Fig. 3.28b, where P_D is the power dissipation, subscript **j** denotes the junction, **c** denotes the case, **s** denotes the heat sink and **a** denotes the ambient.

The total thermal resistance from the junction to ambient is,

$$\Theta_{ja} = \Theta_{jc} + \Theta_{cs} + \Theta_{sa}$$

If the maximum allowable junction temperature T_{jmax} is kept constant for a transistor, the maximum allowable power dissipation P_{Dmax} can be written as,

$$P_{Dmax} = \frac{T_{jmax} - T_a}{\Theta_{ja}}$$

Since P_{Dmax} value is given on specification sheets, it can be considered as constant. If the heat sink is removed, Θ will decrease and T_j and hence P_D will tend to increase that will cause unrecoverable thermal damage on the transistor.

T3. BJT bias stabilization:

There are mainly two types of BJT biasing schemes as shown in Fig. 3.29. The circuit shown in Fig. 3.29a is called the **fixed bias** since $I_B=(V_{CC}-V_{BE})/R_B$ is almost constant. In this circuit, if β is changed, I_{CQ} and hence V_{CEQ} will also change directly. The other configuration, given in Fig. 3.29b, has R_E resistance which increase the stability by the feedback mechanism. The best of all, as far as stability is concerned, is given in Fig. 3.29c. This scheme is called as the **self bias** or the **universal bias** (also called as the voltage divider bias, or the four resistor bias) with R_E. This circuit will result in a Q-point which is almost β independent.

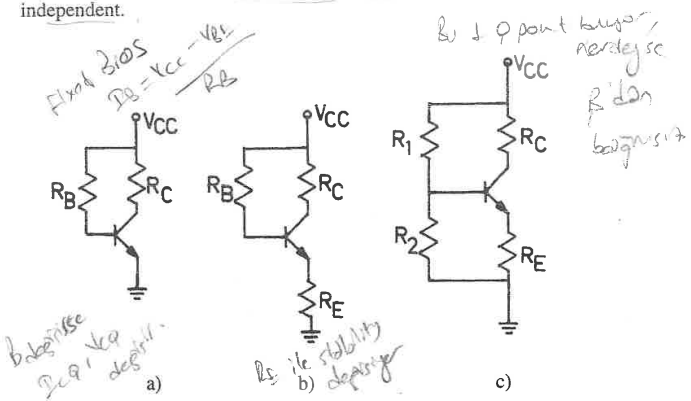


Fig. 3.29 BJT bias types, a) fixed bias, b) fixed bias with R_E, c) self bias with R_E.

PRELIMINARY:

P1. Derive expressions for the stability factors S_V, S_I and S_β for each circuit given in Fig. 3.29. Compare the results with each other and deduce which is more stable. Use the partial derivative method for S_V and S_I, and $S_\beta=\Delta I_{CQ}/\Delta\beta$.

EXPERIMENTAL PROCEDURE:

■ Test your BJT using DMM in KΩ range.

E1. Fixed bias without emitter degeneration:

a) Connect the circuit of Fig. 3.30a.

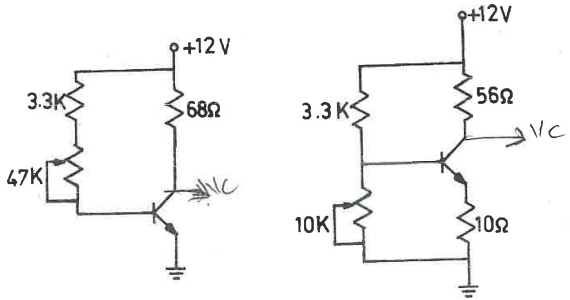
b) With the heat sink mounted on the BJT, adjust the pot to set V_C=6 V (measure with DMM).

c) Remove the heat sink, observe and note the change in I_C with time (fill in Table 3.3 during 1 minute of time with 10 sec. steps).

d) Place the heat sink on the BJT again and observe and note the change in I_C with time, as in part c.

time (sec)>	0	10	20	30	40	50	60
I_C (without heat sink)	7	7,2	7,6	7,8	8,1	8,3	8,5
I_C (with heat sink)	6,3	6,5	6,6	6,61	6,5	6,6	6,7

Table 3.3 Data for the change in I_C with time (fixed bias).



a) b)

Fig. 3.30 a) Fixed bias, b) self bias with R_E.

E2. Self bias with emitter degeneration:

Repeat the procedure E1 for the circuit given in Fig. 3.30b and fill in Table 3.4.

time (sec)>	0	10	20	30	40	50	60
I_C (without heat sink)	5,6	5,7	5,9	6,0	6,0	6,0	6,1
I_C (with heat sink)	5,7	5,7	5,7	5,7	5,7	5,7	5,7

Table 3.4 Data for the change in I_C with time (self bias with R_E).

CONCLUSIONS:

C1. Which configuration in Fig. 3.30 is more stable against the variations in temperature? Why?

C2. What is the purpose of using heat sink?

EQUIPMENT LIST:

Resistors [3.3 K, and 10, 56, 68 (all 0.5 Watt)]Ω

Potentiometers (10 K, 47 K)Ω

BJT (2N221-npn)

Standard set equipment.

EXPERIMENT

8

JUNCTION FIELD EFFECT TRANSISTOR (JFET) FAMILIARIZATION AND CHARACTERISTICS

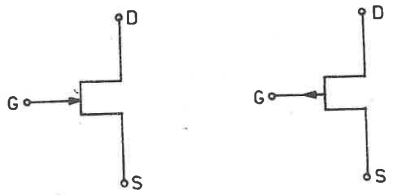
OBJECTIVE:

To become familiar with Junction Field Effect Transistors (JFET) and to investigate the output (drain) and transfer (transconductance) characteristics of JFETs.

THEORY:

T1. Introduction to JFET:

Although it is another three terminal transistor, the physical structure of a JFET is different from that of a BJT. A BJT is a two-junction device whereas a JFET is a unipolar device since its action depends only on one type of charge carriers (i.e. electrons or holes).



a) b)

Fig. 3.31 Symbol for JFET a) n-channel, b) p-channel.

Figure 3.31a illustrates an **n-channel** JFET whose elements are called the source (S), the drain (D) and the gate (G). As the name implies, the channel between the drain and source is made of n-type material in an n-channel JFET and gate is p-type. The opposite types are true for the **p-channel** JFET shown in Fig. 3.31b.

There are many differences between the operation of JFETs and BJTs. The main operational difference is that, the drain current (I_D) in a JFET is controlled by the gate-to-source voltage (V_{GS}), whereas the collector current (I_C) in a BJT is controlled by the base current (I_B). The operation of a JFET is based on the reverse V_{GS} voltage as follows: As the reverse voltage V_{GS} is increased, the number of immobile carriers near the gate increases as well. This process starts to decrease the effective width of the channel. For simplicity, one may consider the channel as a water channel and the reverse V_{GS} voltage as a valve. As the

reverse V_{GS} voltage is increased (i.e. the valve is closed), the drain current decreases (similar to the water flowing through the channel). At the end, the channel will be completely closed and no current (water) flows through. The voltage which makes the channel closed is called $\mathbf{V_{GS(off)}}$ or the **pinch-off voltage** $\mathbf{V_p}$ (be careful that V_p is given as $-V_{GS(off)}$ in some books). On the other hand, when the gate is shorted to the source (this corresponds to $V_{GS}=0$), the current flowing through the channel will be maximum and is called as $\mathbf{I_{DSS}}$. Both I_{DSS} and V_p for a JFET are constant and independent from the external circuitry.

T2. JFET operating regions:

1. Cutoff (Pinch-off) region: Since $|V_{GS}|>|V_p|$, the channel is completely closed and no current flows through ($I_D=0$). In this case, the channel between the drain and source can be assumed as open circuit in DC analysis.

2. Ohmic region: JFETs operating in this region (small V_{DS}) can be used as a **voltage-controlled resistor, VCR** (also called as **voltage-variable resistor, VVR**). In this region, I_D current is dependent on the V_{GS} and V_{DS} voltages as,

$$I_D = \frac{I_{Dss}}{V_p^2}\left[\, 2(V_{GS} - V_p)\, V_{DS} - V_{DS}^2 \,\right]$$

If $|V_{DS}|<<|V_p-V_{GS}|$ then V_{DS}^2 in this equation can be neglected and,

$$I_D = \frac{2\, I_{Dss}}{V_p^2}\,(V_{GS} - V_p)\, V_{DS}$$

which is a linear relation between I_D and V_{DS} as long as V_{GS} is kept constant. The resistance between the drain and source can be written as,

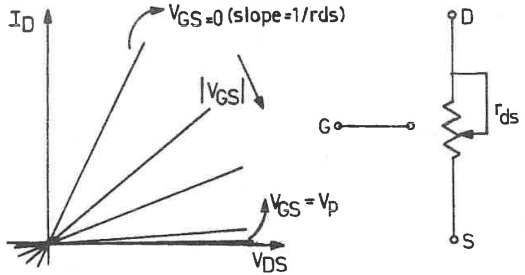
$$R_{DS} = \frac{V_{DS}}{I_D} = \frac{V_p^2}{2\, I_{Dss}\,(V_{GS} - V_p)}$$

Typical drain characteristics for different V_{GS} values and the DC equivalent circuit in the ohmic region are given in Fig. 3.32.

Region	*Biasing of gate*	*Relation between V_{GS}, V_p and V_{DS}*	*I_D (=I_S) I_G=0 always*
active	reverse	$V_{DS}>(V_{GS}-V_p)>0$	$I_{DSS}(1-V_{GS}/V_p)^2$
ohmic	reverse	$(V_{GS}-V_p)>V_{DS}>0$	$(I_{DSS}/V_p^2)[2(V_{GS}-V_p)V_{DS} -V_{DS}^2]$
cutoff	reverse	$V_{GS}<V_p$	0

Table 3.5 n-channel JFET operating regions (polarities of voltages will change for p-channel JFET).

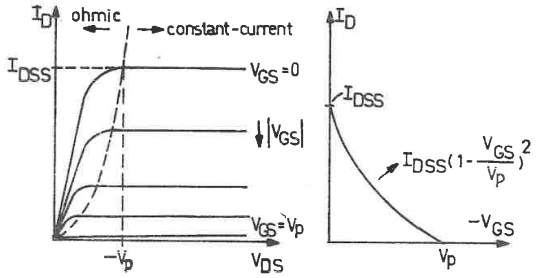
3. Active region: This region is also called the **constant current region** or the **beyond pinch-off region** in some books. In this case, I_D depends on V_{GS} since I_{DSS} and V_p are constant. Typical n-channel JFET drain (output) and transfer (transconductance) characteristics are given in Fig. 3.33. Note from Fig. 3.33a that, as the $|V_{GS}|$ is increased, I_D starts to decrease until $|V_{GS}|=|V_p|$ at which $I_D=0$. A further increase in $|V_{GS}|$ above $|V_p|$ will not change the behavior of the JFET, since the pinch-off has already been reached. The value of V_p can be measured from the characteristic curve given in Fig. 3.33a since it corresponds to the knee voltage after which I_D becomes almost constant, when $V_{GS}=0$. The curve given in Fig. 3.33b is the transfer (or transconductance) characteristics (which is the curve of I_D showing the square power dependence on V_{GS}).



a) b)

Fig. 3.32 JFET a) drain characteristics, b) DC equivalent, in ohmic region.

When $V_{GS}=0$, the channel is open and a maximum current of I_{DSS} can flow through, independent of external circuitry (i.e. if power supply and external resistors allow). A JFET operating in this condition can be used as a constant current source in many applications. A JFET constant current source and its DC equivalent circuit are given in Fig. 3.34.



a) b)

Fig. 3.33 JFET a) drain and b) transfer characteristics.

PRELIMINARY:

P1. Suppose that V_p=-4 V, I_{DSS}=10 mA and V_i=10 V_{p-p} square wave at 100 Hz for the JFET analog switch given in Fig. 3.37. Examine the circuit and draw V_i and V_o on the same scale.

P2. If V_p and I_{DSS} are as given in P1, V_i=5 V_{p-p} square wave at 100 Hz

and the resistor of 1 K is replaced with a capacitor of 1000 μF, draw V_i and V_o on the same scale.

P3. Use the values given in P2 and V_{DD}=(8+4sinωt) V at 10 Hz instead of V_{DD}=12 V, draw V_i and V_o on the same scale for a period of sinωt.

EXPERIMENTAL PROCEDURE:

■ Test your JFET using DMM in KΩ range.

E1. Drain characteristics (in active region):

a) Connect the circuit of Fig. 3.35 and observe the drain (output) characteristics of the n-channel JFET (i.e. I_D-V_{DS} curve) on the CRO.

b) By changing V_{GS} using pot, observe on the CRO that I_D=0. Measure V_{GS} value at this point using DMM. This V_{GS} is V_p of your JFET.

c) Making V_{GS}=0 using pot or simply shorting the gate to the source, measure I_D current with the CRO. This current is the I_{DSS} of your JFET.

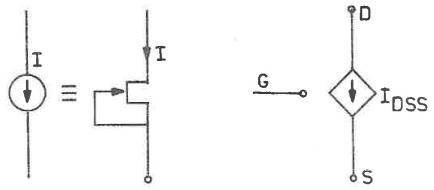
d) Observe and draw the output characteristics for V_{GS}=0, V_p, V_p/4, V_p/2, and V_p. Compare the characteristics with the one given in Fig. 3.33a.

E2. Using JFET as voltage-controlled resistor VCR (in ohmic region):

Use the same set-up that is constructed in E1 to observe the drain characteristics in ohmic region. Just short the diode or simply remove it from the circuit.

a) Set V_i=(0.5sinωt) V at 100 Hz and observe the I_D-V_{DS} curve on the CRO.

b) Observe and draw the VCR characteristics for V_{GS}=0, V_p, V_p/4, V_p/2, and V_p. Compare the characteristics with the one given in Fig. 3.32a.



a) b)

Fig. 3.34 a) JFET constant current source and b) its DC equivalent (V_{GS}=0).

E3. Transfer characteristics (in active region):

a) Connect the circuit of Fig. 3.36 and observe the transfer (transconductance) characteristics (I_D-V_{GS}) of the n-channel JFET on CRO.

b) Observe and draw the I_D-V_{GS} curve on CRO and compare the characteristics with the one given in Fig. 3.33b.

c) Making use of Fig. 3.33b, measure I_{DSS} and V_p of your JFET

on the I_D-V_{GS} curve drawn on part b. Compare the results with the ones obtained in E1.

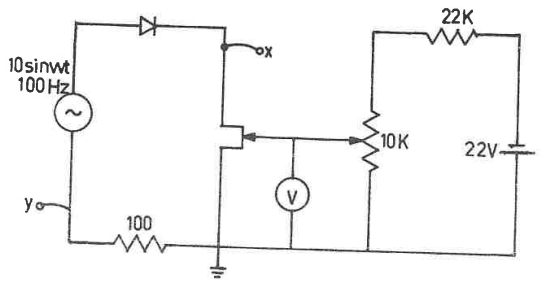


Fig. 3.35 Circuit to obtain drain (output) characteristics of an n-channel JFET.

E4. JFET analog switch:

Knowing that I_D=0 (pinch-off) when $|V_{GS}|>|V_p|$, and $I_D=I_{DSS}$ (saturation) when V_{GS}=0, a JFET can be used as an analog switch as shown in Fig. 3.37. At pinch-off, $V_o=V_{DS}=V_{DD}$ and at saturation $V_o=V_{DS}$=0.

a) Connect the circuit of Fig. 3.37 and adjust V_i=10 $V_{p\text{-}p}$ square wave at 100 Hz.

b) Observe and draw the waveforms on both x (V_i) and y (V_o) inputs of CRO. Compare the results with the ones calculated in P1.

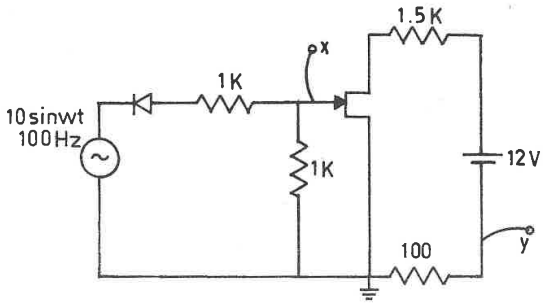


Fig. 3.36 Circuit to obtain transfer (transconductance) characteristics of an n-channel JFET.

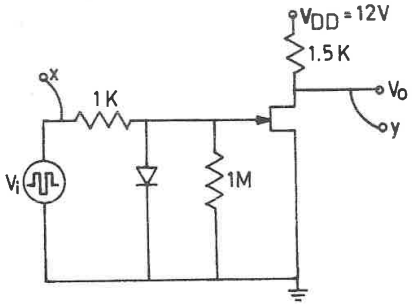


Fig. 3.37 JFET analog switch.

CONCLUSIONS:

C1. What is the function of the diodes in Fig. 3.34 to 3.36?

C2. Draw Fig. 3.34 and 3.35 for the p-channel JFET.

C3. Why did you remove the diode in E2 (Fig. 3.35)?

EQUIPMENT LIST:

Resistors (100, 2*1 K, 1.5 K, 22 K)Ω

Potentiometer (10 K)Ω

Rectifier diode (1N4001)

JFET (BF245 n-channel)

Standard set equipment.

EXPERIMENT

9

JFET BIASING AND AC ANALYSIS

OBJECTIVE:

To examine the basic JFET biasing schemes and to become familiar with the small-signal analysis of JFET circuits.

THEORY:

T1. JFET biasing schemes:

There are mainly three types of JFET biasing circuits as shown in Figure 3.38. The self bias and the voltage divider bias circuits are similar and are advantageous compared to the fixed bias scheme given in Fig. 3.38a since they both require only one voltage source. Because of this reason, the fixed bias scheme is rarely used. The voltage divider bias is the most commonly used scheme since it is the most stable one compared to the other schemes.

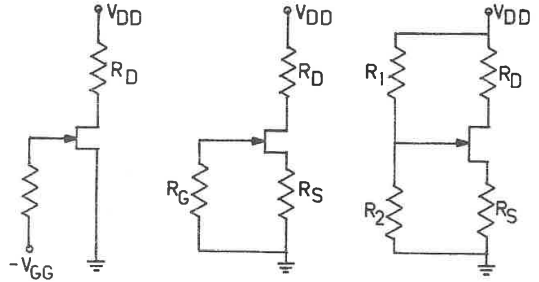
T2. JFET small-signal model:

In the constant current region, a JFET can be modeled as shown

in Figure 3.39. At this operating region,

$$I_D = I_{Dss}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

where I_D is the drain current, V_{GS} is the gate-to-source voltage, V_p is the pinch-off voltage and I_{DSS} is the drain current when V_{GS}=0.



a) b) c)

Fig. 3.38 JFET biasing schemes: a) Fixed bias, b) self bias and c) voltage divider bias. Note that voltage source polarities are given for n-channel JFET.

The small-signal parameters are:

g_m: gate-to-drain transconductance, is equal to the slope of the curve on the I_D versus V_{GS} characteristics for the transistor at the specified operating point.

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}\ constant} = \frac{2\ I_{Dss}}{|V_p|}\left(1 - \frac{V_{GS}}{V_p}\right) = g_{mo}\sqrt{\frac{I_D}{I_{Dss}}}$$

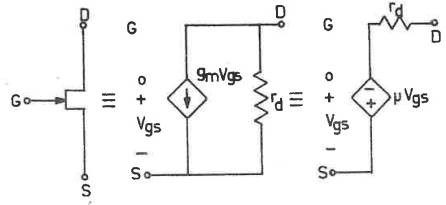


Fig. 3.39 Small-signal model of an n-channel JFET ($\mu=g_m r_d$).

r_d: incremental drain resistance, represents the gradual increase in the drain current with the increasing drain voltage. The value of r_d is equal to the reciprocal of the slope of the I_D versus V_{DS} characteristics for the transistor at the specified operating point. That is,

$$\frac{1}{r_d} \equiv \frac{\partial I_D}{\partial V_{DS}}\Big|_{V_{GS}\ constant}$$

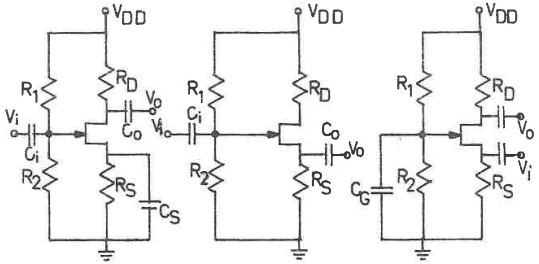
Typical values of r_d lies between 20-500 KΩ.

μ: incremental voltage amplification factor, is given by

$$\mu \equiv \frac{\partial V_{DS}}{\partial V_{GS}} \Big|_{I_D \text{ constant}} = g_m r_d$$

T3. JFET amplifier configurations:

There are three types of JFET amplifier configurations. These are common-source (CS), common-drain (CD) and common-gate (CG) amplifiers as shown in Fig. 3.40. Common-drain is also called as the **source follower**. All of these configurations are biased using the voltage divider configuration given in Fig. 3.38c. The gain and impedance characteristics of each configuration is different from each other. For instance, CS amplifiers have higher voltage gain and nearly infinite input impedance.



a) b) c)

Fig. 3.40 JFET amplifier configurations, a) CS, b) CD and c) CG (C refers to common).

PRELIMINARY:

P1. Given that R_1=10 K, R_S=1 K for the circuit given in Fig. 3.40a. Calculate R_2 and R_D if I_{DSS} =10 mA, V_p = -3 V, V_{DD} =12 V, V_{GSQ}= -1.5 V, and V_{DSQ}=5 V. Draw AC and DC load lines. Draw another AC load line assuming the by-pass capacitor C_S is removed.

EXPERIMENTAL PROCEDURE:

■ Test your JFET using DMM in KΩ range (consider gate as anode of a diode whose cathodes are both drain and source).

E1. Connect the circuit of Fig. 3.40a with the values given and calculated in P1. Measure I_{DQ}, V_{DSQ} and V_{GSQ}. Compare the measured values with the theoretical ones calculated in P1. Take C_i=C_o=100 μF and C_S=470 μF.

E2. Using the low output (LO) of signal generator and the voltage divider circuit given in Fig. 3.41, adjust V_i=(0.1sinωt) V. Measure V_i and V_o on CRO and increase the input voltage until the maximum undistorted output signal is reached (i.e. the output must remain sinusoidal since input is sinusoidal). Record the values of V_i and V_o and calculate the voltage gain (V_o/V_i).

E3. Disconnect the by-pass capacitor C_S and repeat E2. Note the effect of this capacitor if any.

E4. Change the output terminal from the drain to the source as in Fig. 3.40b (so CD configuration is set up) and Repeat E2.

E5. Change the placement of the input and output terminals and add C_G=470 μF as in Fig. 3.40c (so CG configuration is set up) and Repeat E2.

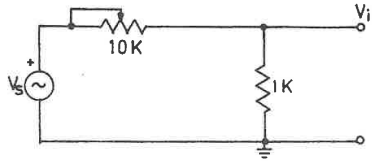


Fig. 3.41 A simple voltage divider to obtain smaller voltages.

CONCLUSIONS:

C1. Compare the theoretical and experimental results obtained in the experiment (P1 and E1). Explain any differences if exist.

C2. Compare the voltage gain of three amplifier configurations given in Fig. 3.40.

C3. What is the effect of C_S in common-source amplifier?

EQUIPMENT LIST:

Resistors (470, 2*1 K, 1.5 K, 1.8 K, 10 K)Ω

Potentiometer (10 K)Ω

Capacitors (2*100, 470)μF

JFET (BF245 n-channel)

Standard set equipment.

EXPERIMENT

10

BJT AC ANALYSIS

OBJECTIVE:

To examine the small-signal BJT amplifier configurations.

THEORY:

T1. BJT small-signal model:

The collector, base and emitter currents (DC) of a BJT operating in active region can be written as,

$$I_E = I_C + I_B$$

$$I_C = \beta I_B + I_{CEO}$$

where β is the DC current gain and I_{CEO} is the collector-to-emitter leakage current. If leakage current is ignored, $I_C = \beta I_B$.

The small-signal equivalent of a BJT can be represented in terms of h-parameters, as shown in Fig. 3.42a. Generally, hre and hoe are

ignored and dynamic (AC) current gain hfe (sometimes denoted as β_{ac}) is assumed to be equal to the DC current gain β (also called β_{dc}). In this case, the simplified small-signal equivalent can be shown as in Fig. 3.42b (β-model) or as in Fig. 3.42c (g_m-model). In these figures, g_m stands for the **transconductance** and r_π is used instead of hie (i.e. r_π=hie). The only difference between Fig. 3.42b and 3.42c is the form of the dependent source parameter. The dependent source parameters in these figures can be related as,

$$i_b = \frac{V_{be}}{r_\pi}$$

$$g_m = \frac{\beta}{r_\pi}$$

$$\beta i_b = g_m V_{be} = \frac{\beta}{r_\pi} V_{be}$$

In addition, r_π is related to DC collector current I_C as,

$$r_\pi = \frac{kT/q}{I_{CQ}/\beta} = \frac{V_T}{I_{BQ}}$$

where k is the Boltzman constant, T is the temperature, q is the electron charge and V_T is the thermal voltage which is about 25 mV at room temperature.

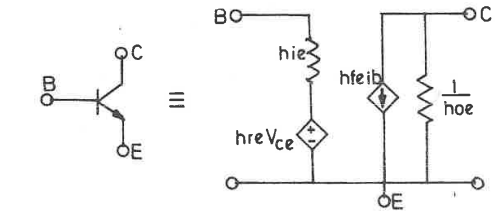


Fig. 3.42 Small-signal model of an npn BJT. a) complete h-model, b) β-model, and c) g_m-model ($\beta=g_m r_\pi$).

T2. BJT amplifier configurations:

There are three types of BJT amplifier configurations. These are common-emitter (CE), common-collector (CC) and common-base (CB) amplifiers as shown in Fig. 3.43. Common-collector configuration is also called as the **emitter follower** since $V_i \approx V_o$. All of these configurations

E5. Change the placement of the input and output terminals and add C_G=470 μF as in Fig. 3.40c (so CG configuration is set up) and Repeat E2.

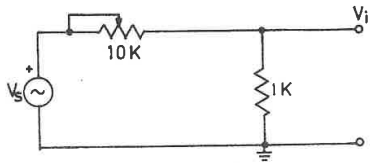


Fig. 3.41 A simple voltage divider to obtain smaller voltages.

CONCLUSIONS:

C1. Compare the theoretical and experimental results obtained in the experiment (P1 and E1). Explain any differences if exist.

C2. Compare the voltage gain of three amplifier configurations given in Fig. 3.40.

C3. What is the effect of C_S in common-source amplifier?

EQUIPMENT LIST:

Resistors (470, 2*1 K, 1.5 K, 1.8 K, 10 K)Ω

Potentiometer (10 K)Ω

Capacitors (2*100, 470)μF

JFET (BF245 n-channel)

Standard set equipment.

EXPERIMENT

10

BJT AC ANALYSIS

OBJECTIVE:

To examine the small-signal BJT amplifier configurations.

THEORY:

T1. BJT small-signal model:

The collector, base and emitter currents (DC) of a BJT operating in active region can be written as,

$$I_E = I_C + I_B$$

$$I_C = \beta I_B + I_{CEO}$$

where β is the DC current gain and I_{CEO} is the collector-to-emitter leakage current. If leakage current is ignored, $I_C = \beta I_B$.

The small-signal equivalent of a BJT can be represented in terms of h-parameters, as shown in Fig. 3.42a. Generally, hre and hoe are

ignored and dynamic (AC) current gain hfe (sometimes denoted as β_{ac}) is assumed to be equal to the DC current gain β (also called β_{dc}). In this case, the simplified small-signal equivalent can be shown as in Fig. 3.42b (β-model) or as in Fig. 3.42c (g_m-model). In these figures, g_m stands for the **transconductance** and r_π is used instead of hie (i.e. r_π=hie). The only difference between Fig. 3.42b and 3.42c is the form of the dependent source parameter. The dependent source parameters in these figures can be related as,

$$i_b = \frac{V_{be}}{r_\pi}$$

$$g_m = \frac{\beta}{r_\pi}$$

$$\beta i_b = g_m V_{be} = \frac{\beta}{r_\pi} V_{be}$$

In addition, r_π is related to DC collector current I_C as,

$$r_\pi = \frac{kT/q}{I_{CQ}/\beta} = \frac{V_T}{I_{BQ}}$$

where k is the Boltzman constant, T is the temperature, q is the electron charge and V_T is the thermal voltage which is about 25 mV at room temperature.

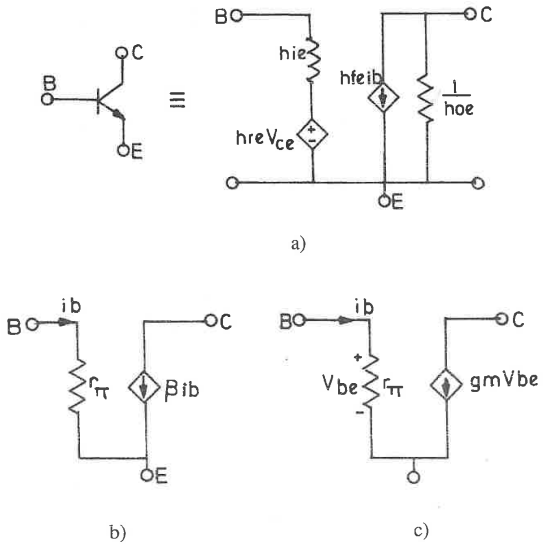
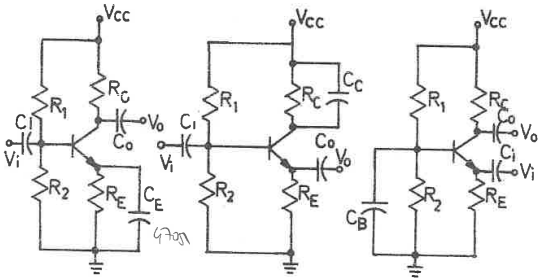


Fig. 3.42 Small-signal model of an npn BJT. a) complete h-model, b) β-model, and c) g_m-model ($\beta=g_m r_\pi$).

T2. BJT amplifier configurations:

There are three types of BJT amplifier configurations. These are common-emitter (CE), common-collector (CC) and common-base (CB) amplifiers as shown in Fig. 3.43. Common-collector configuration is also called as the **emitter follower** since $V_i \approx V_o$. All of these configurations

are biased using the voltage divider configuration. The gain and impedance characteristics of each configuration are different from each other. For example, CE amplifiers have higher voltage gain, CC amplifiers have nearly unity voltage gain, high input impedance and low output impedance. Amplifier configurations are chosen according to these specifications.



a) b) c)

Fig. 3.43 BJT amplifier configurations, a) CE, b) CC and c) CB (C refers to common).

PRELIMINARY:

P1. Calculate R_E to set V_{CEQ}=5.9 V for the circuit given in Fig. 3.43a. Given that R_1=18 K, R_2=5.6 K, R_C=1 K, V_{CC} =12 V, V_{BE}= 0.7 V, and β=100. Draw AC and DC load lines. Calculate the maximum allowable

voltage swing (p-p) at the output.

P2. Draw another AC load line assuming the by-pass capacitor C_E is removed. Calculate the maximum allowable voltage swing (p-p) at the output. What is the difference between the cases in P1 and P2?

EXPERIMENTAL PROCEDURE:

- Test your BJT using DMM in KΩ range.
- Take C_i=C_o=100 μF and C_E=C_C=C_B=470 μF throughout the procedure.

E1. Connect the circuit of Fig. 3.43a with the values given and calculated in P1. Measure I_{CQ} and V_{CEQ}. Compare the measured values with the theoretical ones that you calculated in P1.

E2. Using the low output (LO) of the signal generator and the voltage divider circuit given in Fig. 3.41, adjust V_i=(0.1sinωt) V. Measure V_i and V_o on CRO and increase the input voltage until the maximum undistorted output signal is obtained (i.e. the output must remain sinusoidal since input is sinusoidal). Record the values of V_i and V_o and calculate the voltage gain (V_o/V_i).

E3. Disconnect the by-pass capacitor C_E and repeat E2. Note the effect of this capacitor if any.

E4. Change the output terminal from the collector to the emitter and connect C_C as in Fig. 3.43b (so CC configuration is set up). Repeat E2.

E5. Change the placement of the input and output terminals and add C_B=470 μF as shown in Fig. 3.43c (so CB configuration is set up).

Repeat E2.

CONCLUSIONS:

C1. Compare the theoretical and experimental results obtained in the experiment (P1 and E1). Explain any differences if exist.

C2. Compare the voltage gain of three amplifier configurations given in Fig. 3.43.

C3. What is the effect of C_E in the common-emitter amplifier?

EQUIPMENT LIST:

Resistors (470, 2*1 K, 5.6 K, 18 K)Ω

Potentiometer (10 K)Ω

Capacitors (2*100, 470)μF

BJT (BC237 npn)

Standard set equipment.

EXPERIMENT

11

COMPOUND AMPLIFIERS

OBJECTIVE:

To investigate the properties of Darlington and complementary BJT compound amplifiers.

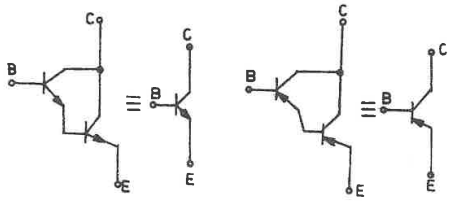
THEORY:

There are two basic types of BJT compound amplifiers, namely, Darlington pair and complementary.

T1. Darlington configuration:

The Darlington pair consists of two devices in a compound configuration. This configuration yields an overall α close to unity which means very high β on the order of 1000, or more.

Some manufacturers package the Darlington pair as a single composite device having only three external leads. The Darlington configuration not only supports a higher current gain, but also a higher input impedance compared with a single transistor configuration.



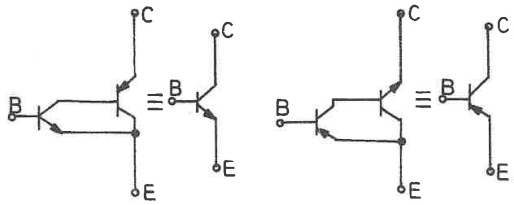
a) b)

Fig. 3.44 Darlington connected BJT pairs and their single transistor equivalents. a) npn type, b) pnp type.

T2. Complementary configuration:

The other compound configuration, the complementary type, is shown in Fig. 3.45. In this amplifier, the transistor types alternate from npn to pnp. The collector current of the first transistor is the base current of the second, so the total current gain may be approximately equal to the product of βs of the transistors used. In contrast to Darlington configuration, the input resistance of this amplifier is equal to that of the first transistor.

In addition to the Darlington and complementary configurations, there are many other two-transistor combinations which are not taken into account in this experiment.



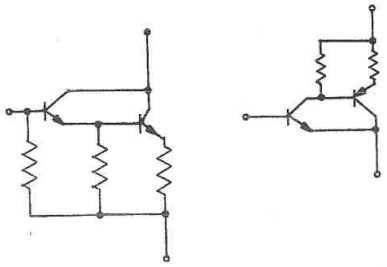
a) b)

Fig. 3.45 Complementary connected BJT pairs and their single transistor equivalents. a) npn type, b) pnp type.

T3. Practical Remarks:

- It should be noted that the second transistor in the compound connection should have a base current rating which is greater than or equal to the collector (or emitter) current of the first stage (i.e. second transistor must have a higher power rating).
- For the complementary compound BJTs, by using alternate types for the first and second transistors, either npn or pnp type composite transistors maybe obtained as shown in Fig. 3.45.
- One problem that may arise in the compound configuration results from the I_{CEO} of T1. It is first multiplied by the stability factor of T1, then enters the base of T2, and then multiplied by the current gain of T2. If germanium transistors are used, the component of the leakage current may be prohibitively large. This current can be greatly reduced

at the expense of reduced current gain if the linear stabilization circuits of Fig. 3.46 are used.



a) b)

Fig. 3.46 Linear stabilization circuits for a) Darlington and b)complementary configurations.

PRELIMINARY:

P1. Determine the equivalent h-parameters of the configurations shown in Fig. 3.44a and Fig. 3.45a (omit hoe and hre, use only hie and β=hfe).

P2. Given that V_{BE1}=0.6 V, V_{BE2}=0.65 V, β_1=200, β_2=120 for the circuit of Fig. 3.47. Calculate:

a) I_{CQ} and V_{CEQ} for each transistor,

b) the DC voltage drop on each resistor,

c) the voltage gain ($A_V=V_o/V_i$) and current gain ($A_I=i_o/i_i$),

d) the input and output resistances (look from V_i to find R_i and from V_o to find R_o).

P3. Repeat P2 for the circuit of Fig. 3.48.

EXPERIMENTAL PROCEDURE:

- Check your transistors using DMM.
- Use C_i=22 μF, C_o=100 μF, C_E=220 μF and 1 KHz input signal from the low output (LO) of the signal generator throughout the procedure.

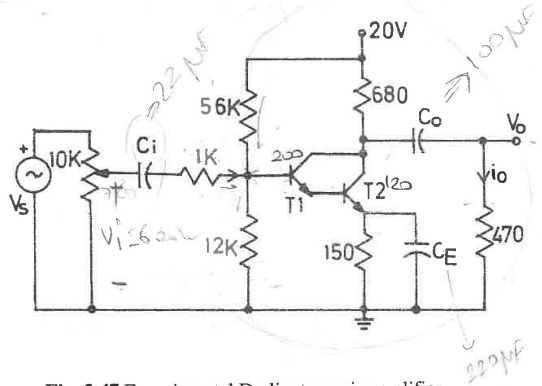


Fig. 3.47 Experimental Darlington pair amplifier (T1:BC237, T2:BD135).

E1. Construct the circuit illustrated in Fig. 3.47.

a) Measure and record I_{CQ} and V_{CEQ} of each transistor. Also measure the DC voltage drop on each resistor.

b) Adjust the input signal amplitude using the amplitude pot on SG and 10 K pot at the input, to find the maximum input signal that

results in the maximum undistorted output.

c) Keeping the input signal unchanged, measure the amplitudes of the input and output waveforms with CRO and calculate the voltage and current gain of the whole circuit.

HINT: To calculate the current gain, measure the input and output currents with CRO, i.e. the voltage drop on 1 K resistor divided by 1 K will give input current and the output voltage divided by 470 Ω will give the output current.

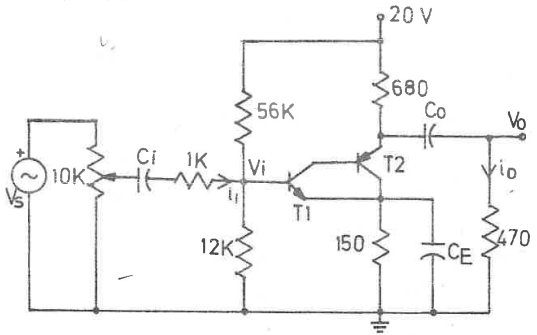


Fig. 3.48 Experimental complementary amplifier (T1:BC237, T2:BD136).

d) Calculate R_i using the AC input voltage and current values measured in part c.

e) R_o can be measured indirectly in the following way.

Disconnect R_L from the circuit and measure the open output voltage $V_{o(open)}$. Connect the 10 K pot at the output. Adjust the pot slowly until the output voltage is to be $V_{o(open)}/2$. Disconnect the pot and measure its resistance which is R_o.

E2. Construct the circuit illustrated in Fig. 3.48 and repeat the procedure E1 for this circuit.

CONCLUSIONS:

C1. Compare the theoretical and experimental results. If there exists some differences, explain the possible reasons for them.

C2. What is the purpose of using C_E in Fig. 3.47 and 3.48?

EQUIPMENT LIST:

Potentiometer (10K)Ω

Resistors (150, 470, 680, 1 K, 12K, 56K)Ω

Capacitors (22, 100, 220)μF (all 25 V or greater)

Transistors (BC237 npn, BD135 npn, BD136 pnp)

Standard set equipment.

EXPERIMENT

12

DIFFERENTIAL AMPLIFIERS

OBJECTIVE:

To investigate the properties of the BJT differential amplifiers.

THEORY:

The basic feature of the differential amplifiers (also called **difference amplifiers**) is the ability to yield output which is proportional to the difference between the inputs. Fig. 3.49 shows the simplest form of a differential amplifier.

The output can be taken in a differential form (double-ended) from terminals V_{o1} and V_{o2}, or in single-ended form from the terminal V_{o1} or V_{o2}. Assume that single-ended output signal is taken from V_{o2} terminal whose voltage with respect to ground can be written as

$$V_{o2} = A_{cm} V_{cm} + A_{dm} V_{dm}$$

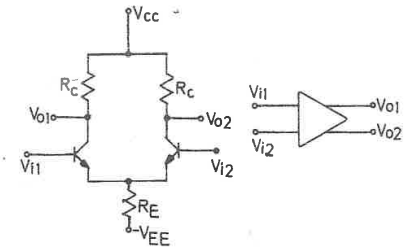
where subscripts *dm* and *cm* denote differential-mode and common-mode, respectively.

The common-mode and differential-mode inputs signals are defined as

$$V_{cm} = \frac{V_{i1} + V_{i2}}{2}, \qquad V_{dm} = V_{i1} - V_{i2}$$

Differential mode gain in the case when the output is taken from V_{o2} and V_{o1} can be written as,

$$A_{dm} = \frac{V_{o2} - V_{o1}}{V_{i2} - V_{i1}}$$



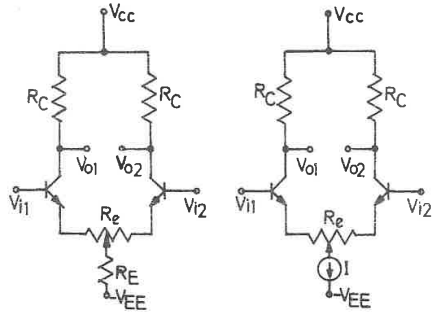
a) b)

Fig. 3.49 Basic differential amplifier, a) circuit schematic, b) block diagram.

One of the most serious problems in differential amplifiers is the common-mode gain. When $V_{i1}=V_{i2}$ (i.e. both inputs are connected to the

same source), ideally the difference between the output V_{o2}-V_{o1} must be zero. However, since the real transistors are not exactly matched, there will be an unwanted amplification for the common mode signals. This gain can be written as,

$$A_{cm} = \frac{V_{o2} - V_{o1}}{2\ V_{in}} \quad where \quad V_{in} = V_{i1} = V_{i2}$$



a) b)

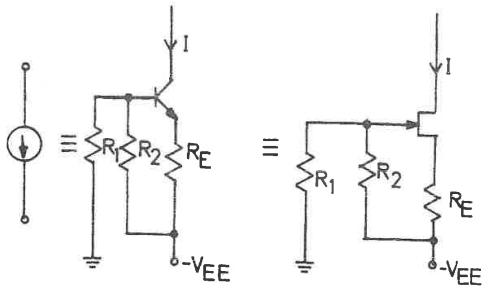
Fig. 3.50 Differential amplifier with a) emitter resistor R_E, b) constant current source.

A_{dm} is usually desired to be high in a differential amplifier. It must be at least some orders of magnitude greater than the common-mode gain A_{cm}. Physically, this means that, differential amplifier

amplifies the difference between the input signals whereas it does not amplify the input signals of the same magnitude. A measure of the quality of the amplifier is the **common mode rejection ratio CMRR**, defined as

$$CMRR = \frac{A_{dm}}{A_{cm}}$$

Practically, the differential amplifier requires matched transistors, but this disadvantage could be avoided to some extent using the emitter resistor R_e (or a rheostat) as shown in Fig. 3.50. To minimize the efforts in design, $-V_{EE}$ source can be included.



a) b)

Fig. 3.51 Constant current source using a) BJT, b) JFET.

To improve CMRR, it is necessary to increase R_E but then I_{E1}

and I_{E2} will decrease causing CMRR to decrease. Therefore, it is more practical to use a current source of the form shown in Fig. 3.51 to obtain higher a CMRR. The constant current source can be realized using BJT or JFET.

PRELIMINARY:

P1. Obtain expressions for A_{dm} and A_{cm} for the circuit of Fig. 3.50a (Hint: Ignore h_{oe} and h_{re} in the small-signal model).

P2. Calculate R_E and R_C of the circuit given in Fig. 3.50a for the following specifications:

- V_{CC}=-V_{EE}=12 V, I_{C1}=I_{C2}=2 mA,
- the maximum DC voltage at the output V_{o2} is 6.6 V,
- BJTs are BC237 (V_{BE}=0.7 V, β=100),
- R_e=500 Ω rheostat (adjusted at its midpoint).

Calculate the voltage gain from each terminal to the corresponding output, i.e.,

$$A_{V1} = \frac{V_{o2}}{V_{i1}}\Big|_{V_{i2}=0} \quad , \quad A_{V2} = \frac{V_{o2}}{V_{i2}}\Big|_{V_{i1}=0}$$

Ignore h_{oe} and h_{re}.

P3. Design a 4 mA constant current source using the BJT configuration shown in Fig. 3.51a. Given that: β=100, V_{BE}=0.7 V, R_E=1 K, R_2=10 K, V_{EE}=12 V. Find R_1 and calculate the effective output resistance seen across collector to -V_{EE} source if h_{oe}=(100 K)$^{-1}$.

P4. Design a 4 mA constant current source using the JFET configuration in Fig. 3.51b. Given that: I_{DSS}=10 mA, V_p=-3 V, R_E=1 K, R_2=10 K, V_{EE}=12 V. Find R_1.

EXPERIMENTAL PROCEDURE:

■ Test your BJTs using DMM in KΩ range using the diode equivalent model of the BJT.

E1. Measure A_{cm}, A_{dm} and CMRR of the circuit you designed in P2 (Fig. 3.50a).

a) take V_{i1}=V_{i2}=[0.5sin(200π)t]V to measure A_{cm},

b) take V_{i2}=0 and V_{i1}=[0.5sin(200π)t]V to measure A_{dm},

c) calculate CMRR using the measured A_{cm} and A_{dm} values,

d) measure the frequency response of A_{dm} using V_{i1}=[0.5sinωt]V with f=20 Hz to 50 KHz (take at least 10 data),

e) observe V_{i1}-V_{o2} and V_{i1}-V_{o1} curves (transfer characteristics) on CRO.

E2. Repeat E1 (parts a to c) for the circuit in Fig. 3.50b with the BJT constant current source given in Fig. 3.51a (Use the parameters calculated in P2 and P3).

CONCLUSIONS:

C1. Compare the theoretical and experimental results obtained in the experiment. Explain any differences if exist.

C2. Compare the CMRR values obtained in E1 and E2. Comment on the

results.

EQUIPMENT LIST:

Resistors (1 K, 3*2.7 K, 10 K, 15 K)Ω

Potentiometer (500 or 470)Ω

Transistors (BJT:3*BC237-npn)

Standard set equipment.

EXPERIMENT

13

OPERATIONAL AMPLIFIER: OPAMP

OBJECTIVE:

To become familiar with OPAMPs, introduction to the OPAMP parameters and their measurement.

THEORY:

An OPAMP is a high gain direct-coupled differential linear amplifier whose response characteristics are externally controlled by negative feedback from output to the input. OPAMPs can perform mathematical operations such as summing, integration, and differentiation. They are also used as audio and video amplifiers, oscillators, active filters etc.

Fig. 3.52a shows the symbol for an OPAMP. (-) input is called **inverting input** and a signal applied to this input will be shifted 180° at the output. (+) input is called as **noninverting input** and a signal applied to this input will have the same phase at the output.

Fig. 3.52b shows the small-signal (non-ideal) OPAMP model. The input and output resistances and open loop gain in this model are

different than the ideal OPAMP parameters. Ideally, OPAMPs have:

$R_i = \infty$ (input resistance),

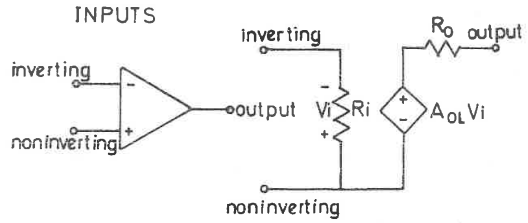
$R_o = 0$ (output resistance),

$A_{OL} = \infty$ (open loop voltage gain),

BW $= \infty$ (bandwidth),

$V_{io} = 0$ (input offset voltage),

and temperature independent characteristics.



a) b)

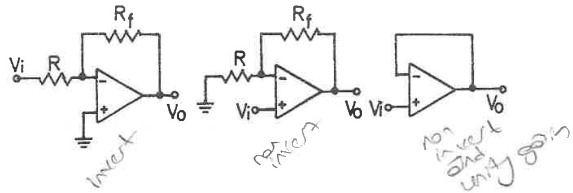
Fig. 3.52 OPAMP a) symbol, b) nonideal model.

T1. Negative feedback:

Fig. 3.53a shows the basic inverting amplifier. Note that the output is fed back to the inverting input in order to provide negative feedback for the amplifier. Since the input is applied to the inverting terminal, the voltage at the output will have (-) sign. The noninverting amplifier shown in Fig. 3.53b also has negative feedback connected to

the inverting terminal. Be careful that for conventional OPAMP applications output is fedback to the inverting input.

The simplest way to analyze the OPAMP circuits is to use nodal analysis approach. Since the input resistance of an ideal OPAMP is assumed to be infinite, no current passes through the input terminals hence one can choose (-) and (+) inputs as separate nodes and write separate node equations for each. Then these node voltages can be equated to each other since they are assumed to be "virtually" grounded. The term virtual denotes that this is not the actual case since the resistance between these terminals is infinite (open circuit). But this assumption is made to denote that the voltages on these terminals are equal (short circuit) although they act as open terminals. Note that we can never write node equations for the output terminal, since the current flowing through the output of OPAMP is not known.



a) b) c)

Fig. 3.53 OPAMP feedback amplifiers: a) inverting, b) noninverting and c) noninverting unity gain (voltage follower).

Since the gain of the configurations in Fig. 3.53 only depends on the resistor values, it is possible to change the gain by changing these resistors. The inverting amplifier shown in Fig. 3.53a has a voltage gain of ($-R_f/R$) whereas the noninverting amplifier shown in Fig. 3.53b has ($1 + R_f/R$). It is also possible to design voltage follower ($V_o=V_i$) shown in Fig. 3.53c with the help of the noninverting amplifier shown in Fig. 3.53b, with $R_f=0$ and $R=\infty$.

The IC OPAMP used in this experiment is type 741 general purpose operational amplifier having the following specifications:

741 OPAMP SPECIFICATIONS:

A_{OL}	20-200 V/mV (R_L>2KΩ , Vo=±10 V) (open loop gain)
R_i	0.3-2 MΩ (input resistance)
R_o	typically 75 (output resistance)
I_B	typically 80 max 500 nA (input bias current)
V_{io}	typically 1 max 6 mV (Rs=10 KΩ)
I_{io}	typically 20 nA (input offset current)
CMRR	typically 30000 (common-mode rejection ratio)
PSRR	typically 10 max 150 μV/V (power supply rejection ratio)
V_{CC}, $-V_{EE}$	max +18 V (supply voltage)
V_i	max ±13 V (input voltage)
V_o	max ±13 V (output voltage)
I_{osc}	typically 25 mA (output short circuit current)
I_{CC}	typically 1.4 max 2.8 mA (supply current)

P_D	typically 50 max 85 mW (dissipated power)

T2. Measurement of OPAMP parameters:

T2.1. I_B (input bias current): I_B is the average current flowing through the inverting and noninverting terminals of an OPAMP. This current flows through the bases of the first stage differential amplifier inside the OPAMP. Fig. 3.54 can be used to measure I_B which can be written as,

$$I_B = \frac{|I_{B-}| + |I_{B+}|}{2}$$

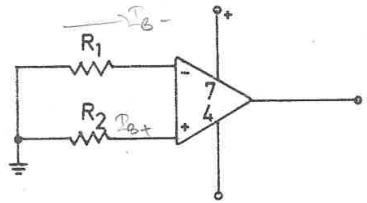


Fig. 3.54 Circuit for measuring I_B.

T2.2. I_{io} (input offset current): I_{io} is the absolute difference between the input bias currents I_{B+} and I_{B-} driven from a common source.

$$I_{io} = |I_{B+}| - |I_{B-}|$$

T2.3. V_{io} (input offset voltage): V_{io} is the differential input voltage between the inverting and noninverting inputs which is needed to make the quiescent output voltage zero.

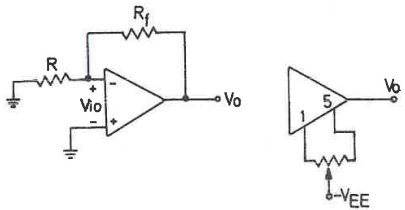
The circuit of Fig. 3.55a can be used to measure V_{io} which can be calculated from the relation,

$$V_o = \frac{R + R_f}{R} V_{io}$$

T2a. V_{io} compensation: Even if the both inputs of an OPAMP are grounded, there still exists an output voltage because $A_{OL}*V_{io}$ product will generally be sufficiently high to saturate the OPAMP. In order to avoid this harmful offset voltage, V_{io} can be compensated using the "offset null" legs (legs 1 and 5 for 741) as shown in Fig. 3.55b.

T2.4. CMRR (common-mode rejection ratio): CMRR is defined as the ratio of the difference-mode gain to the common-mode gain. A higher CMRR is better as explained for differential amplifiers. Fig. 3.56 can be used to measure the CMRR which can be written as,

$$CMRR = \frac{A_{dm}}{A_{cm}} = \frac{V_C}{V_i} = \frac{R + R'}{R} \frac{V_s}{V_o}$$



a) b)

Fig. 3.55 a) Circuit for measuring V_{io}, b) V_{io} compensation.

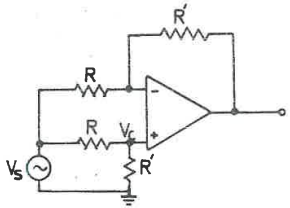


Fig. 3.56 Circuit for measuring CMRR.

T2.5. S_R (slew rate): The slew rate is defined as the maximum rate at which the output voltage can change. S_R can be written as,

$$S_R = \frac{\Delta V}{\Delta t} \left(\frac{Volts}{\mu seconds} \right)$$

It can be measured using the circuit given in Fig. 3.57.

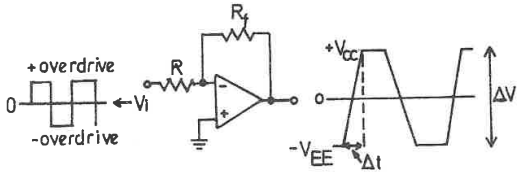
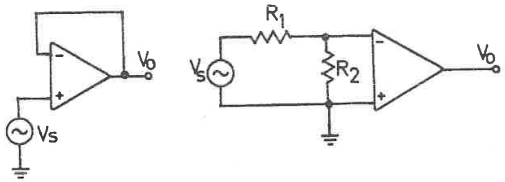


Fig. 3.57 Circuit for measuring slew rate S_R.

T2.6. A_{OL} (open loop gain): A_{OL} is the difference-mode gain of the OPAMP when there is no feedback. It can be measured by the following two methods:



a) b)

Fig. 3.58 Circuits for measuring A_{OL}. a) Unity gain BW method, b) direct method.

A) Gain*Bandwidth method: Since "gain*bandwidth=constant", unity gain bandwidth of OPAMP can be used to calculate the open loop voltage gain A_{OL}. Assuming that the open loop bandwidth BW_{OL} is known (BW_{OL} is about 10 Hz or smaller for 741 OPAMP),

$$A_{CL}\ BW_{CL} = A_{OL}\ BW_{OL}$$

where subscript CL refers to closed loop.

At unity gain (voltage follower), A_{CL}=1, so A_{OL} can be written as,

$$A_{OL} = \frac{BW_{CL}}{BW_{OL}} = \frac{BW_{CL}}{10}$$

BW_{CL} can be assumed as the high cut-off frequency of the closed loop amplifier since the low cut-off frequency is too low. High cut-off frequency is the frequency at which gain reduces from 1 to 0.707 (or from 0 dB to -3 dB). Fig. 3.58a can be used to measure the A_{OL} with this method.

B) Direct method: Another method to measure A_{OL} incorporates the direct measurement at which the open loop OPAMP amplifier is driven by a small voltage as shown in Fig. 3.58b. The accuracy of this method is not good enough since the V_{io} compensation at open loop is almost impossible. A_{OL} can be written as,

$$A_{OL} = \frac{V_o}{V_-} \quad where \quad V_- = \frac{R_2}{R_1 + R_2} V_s$$

EXPERIMENTAL PROCEDURE:

E1. Measurement of I_B and I_{io}:

a) Construct the circuit of Fig. 3.54 with R_1=R_2=11 MΩ. Measure the exact values of resistors R_1 and R_2 with DMM before connecting to the circuit.

b) Measure the voltages on R_1 and R_2 with CRO.

c) Dividing these voltages to the corresponding resistor calculate I_{B+} and I_{B-}, then calculate average of them (i.e. I_B).

d) Calculate I_{io} from the data obtained in E1c.

E2. Measurement of V_{io}:

a) Construct the circuit of Fig. 3.55a with R=100Ω and R_f=100 K.

b) Measure V_o with CRO and calculate V_{io} using the relation given in T2.3.

E3. Compensation of V_{io}: Keeping the circuit given in Fig. 3.55a unchanged,

a) Connect a pot between the legs 1 and 5 of 741 as shown in Fig. 3.55b (while Fig. 3.55a remain unchanged).

b) Adjust the pot until V_o=0.

■ When these steps are completed, V_{io} has been compensated. Do not change the pot until the end of the experiment unless otherwise stated.

E4. Construct the circuit of Fig. 3.56 with R=100, R'=100 K and V_s=(2sinωt) V. Measure V_o and calculate CMRR using the formula given in T2.4.

E5. Construct the circuit of Fig. 3.57 with R=10 K and R_f=100 K. Measure Δt and ΔV and calculate S_R from the formula given in T2.5.

E6. Construct the circuit of Fig. 3.58a.

a) Use V_s=(2sinωt) V at 100 Hz.

b) Measure V_o with CRO while increasing the frequency of the source until you read 2*0.707=1.4 V at the output.

c) Read the frequency of the V_s which is the high cut-off frequency (or BW_{CL}) of OPAMP for this configuration. Calculate A_{OL} using the relation given above.

Attention: Procedure steps from E6 to E8 give uncertain results because of the nonideal behavior of the OPAMP and are left to students choice to follow.

E7. Direct measurement of A_{OL}:

a) Construct the circuit of Fig. 3.58b with R_1=11 MΩ and R_2=10 KΩ.

b) Adjust 12 V>V_s>1 Volts and f<10 Hz or DC.

c) Measure V_s and V_o by both inputs of CRO and, calculate V- and A_{OL} using the relations given in T2.6b.

E8. Measurement of output resistance R_o:

a) Connect the circuit of Fig. 3.58b with R_L=1 KΩ at the output and measure V_o.

b) Calculate R_o using the output stage equivalent circuit of the OPAMP shown in Fig. 3.59.

E9. Measurement of input resistance R_i:

a) Connect the input stage of the circuit of Fig. 3.59 with R=11MΩ (keep output open).

b) Use 12 V>V_s>1 V and f<10 Hz or DC.

c) Measure V- and calculate R_i with the help of OPAMP input stage equivalent in Fig. 3.59.

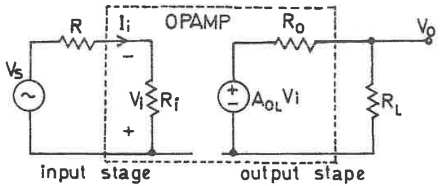


Fig. 3.59 Nonideal OPAMP equivalent for calculation of R_i and R_o.

CONCLUSIONS:

C1. Compare the data obtained in the experiment and the ones given for 741 OPAMP. Explain any differences if exist.

C2. What is the purpose of using voltage follower?

EQUIPMENT LIST:

Resistors (2*100, 1 K, 10 K, 2*100 K, 2*11 M)Ω

Potentiometer (5 K)Ω

IC OPAMP (LM741)

Standard set equipment.

EXPERIMENT

14

LINEAR OPAMP CIRCUITS

OBJECTIVE:

Introduction to the basic linear OPAMP circuits.

THEORY:

T1. Voltage comparator:

A simple voltage comparator circuit is shown in Fig. 3.60. Since no feedback is employed, a small voltage difference between the inputs of the OPAMP results in a saturated output (i.e. $V_o \approx V_{CC}$ or $-V_{EE}$ depending on the input). Since V-=0,

$$V_i = V_+ - V_- = V_+$$

meaning that $V_o>0$ if $V_i>0$ (red LED is ON) and, $V_o<0$ if $V_i<0$ (green LED is ON). V+ and zero are compared in this example. One can connect a voltage source to V- (instead of grounding it) and compare the V+ and V- voltages.

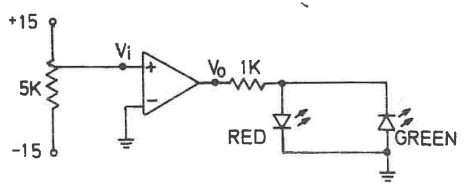


Fig. 3.60 Voltage comparator.

T2. Noninverting amplifier:

The output voltage of the noninverting amplifier shown in Fig. 3.61 can be written as,

$$V_o = \left(1 + \frac{R_f}{R} \right) V_s$$

which shows that amplifier gain can simply be adjusted by proper choose of R_f and R.

T3. Inverting amplifier:

The output voltage of the inverting amplifier shown in Fig. 3.62 can be written as,

$$V_o = - \frac{R_f}{R} V_s$$

Similar to the noninverting amplifier, amplifier gain can be changed if R_f and/or R is changed.

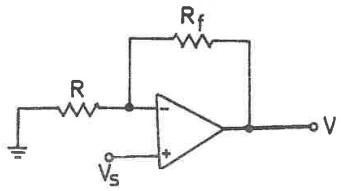


Fig. 3.61 Noninverting amplifier.

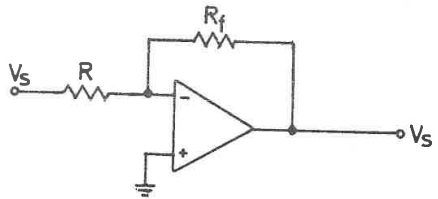


Fig. 3.62 Inverting amplifier.

T4. Summing amplifier:

The output voltage of the summing amplifier shown in Fig. 3.63 can be written as,

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 \right)$$

If R_f, R_1 and R_2 is chosen such that $R_f=R_1=R_2$,

$$V_o = -(V_1 + V_2)$$

which is the sum of the inputs with reversed polarity.

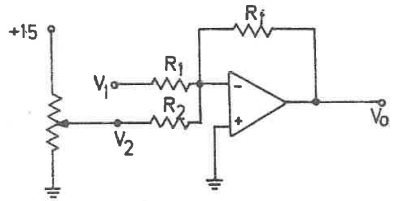


Fig. 3.63 Summing amplifier.

T5. Subtracting amplifier:

The output voltage of the subtracting amplifier shown in Fig. 3.64 can be written as,

$$V_o = -\frac{R_f}{R_1} V_1 + \frac{R_3}{R_2 + R_3}\left(1 + \frac{R_f}{R_1} \right) V_2$$

If $R_f=R_1$ and $R_2=R_3$,

$$V_o = (V_2 - V_1)$$

which is the difference of the inputs.

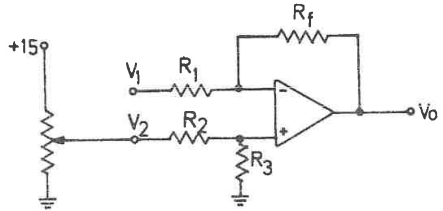


Fig. 3.64 Subtracting amplifier.

T6. Diode tester:

The circuit given in Fig. 3.65 can be used as diode tester (rectifier, zener or LED). If the rectifier diode is connected to the circuit as shown, V_o will be equal to $-V_\gamma$, if zener is connected as given direction, V_o will be $-V_Z$.

PRELIMINARY:

P1. Verify the V_o equations given for T1 to T6, writing node equations for ideal OPAMP model.

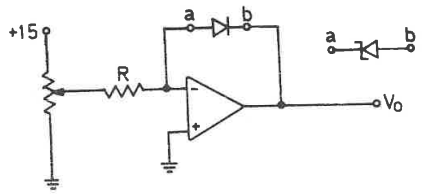


Fig. 3.65 Diode tester.

EXPERIMENTAL PROCEDURE:

E1. Connect the circuit of Fig. 3.60. By adjusting the pot, observe that the red LED is on when $V_i>0$, and the green one is on when $V_i<0$.

E2. Connect the circuit of Fig. 3.61 with R=1 K, R_f=10 K and V_s=1 V. Observe V_o on the CRO. Hint: Get 1 V from SG at DC position.

E3. Connect the circuit of Fig. 3.62 with R=1 K, R_f=10 K and V_s=1 V. Observe V_o on CRO.

E4. Connect the circuit of Fig. 3.63 with $R=R_1=R_f$=10 K.

a) Adjust V_2=3 V using pot.

b) Set V_1=1 V and observe V_o on CRO.

c) Set $V_1=(1\sin\omega t)$ V at 100 Hz and observe V_o on CRO.

E5. Connect the circuit of Fig. 3.64 with $R_1=R_2=R_3=R_f$=10 K.

a) Adjust V_2=3 V using pot.

b) Set V_1=1 V and observe V_o on CRO.

c) Set $V_1=(1\sin\omega t)$ V at 100 Hz and observe V_o on CRO.

E6. Connect the circuit of Fig. 3.65 with R=10 K.

a) Test the rectifier diode (if V_o=-V_γ the diode is O.K.).

b) Replace the rectifier diode with the zener as the same direction as given in Fig. 3.65. Test the zener diode (if V_o=-V_Z diode is O.K.).

CONCLUSIONS:

C1. Compare the experimental and theoretical results. Comment on the differences between them if exists.

EQUIPMENT LIST:

Resistors (1 K, 4*10 K)Ω

Potentiometer (5 K)Ω

Rectifier diode (1N4001)

LED (RED and GREEN)

Zener diode [BZX8506V2 (6.2 V)]

IC OPAMP (LM741)

Standard set equipment.

EXPERIMENT

15

NONLINEAR OPAMP CIRCUITS

OBJECTIVE:

Introduction to the nonlinear OPAMP circuits.

THEORY:

T1. Integrator:

A simple integrator circuit incorporating OPAMP is shown in Fig. 3.66a. The output can be written as,

$$V_o = \frac{(-1)}{RC} \int V_s \, dt$$

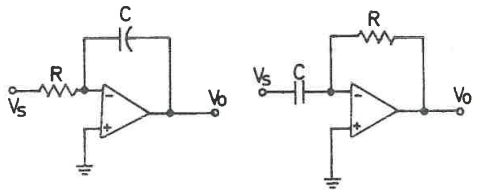
which is the integral of the input.

T2. Differentiator:

A simple OPAMP differentiator circuit is shown in Fig. 3.66b. The output can be written as,

$$V_o = - RC \frac{dV_s}{dt}$$

which is the derivative of the input.

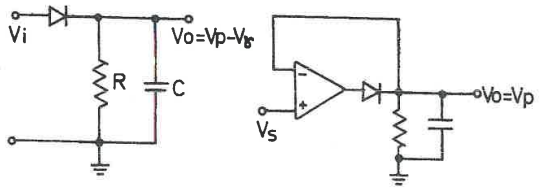


a) b)

Fig. 3.66 OPAMP a) integrator, b) differentiator.

T3. Active peak detector:

In a passive peak detector as shown in Fig. 3.67a, the diode barrier voltage V_γ restricts the input voltage to be lower than that value. If, on the other hand, voltages less than V_γ are needed to be detected, the active peak detector shown in Fig. 3.67b must be used. In this configuration, the effective value of diode barrier voltage is reduced by a factor of A_{OL} and if $V_i \geq V_\gamma/A_{OL}$, $V_o=V_i$. For example, if a silicone rectifier diode of $V_\gamma=0.7$ V is used in a passive peak detector, V_o will be zero for Vi<0.7 V. In the case of active peak detector with the same diode and an OPAMP with $A_{OL}=10^5$, when $V_i \geq 7\ \mu V$, $V_o=V_i$.

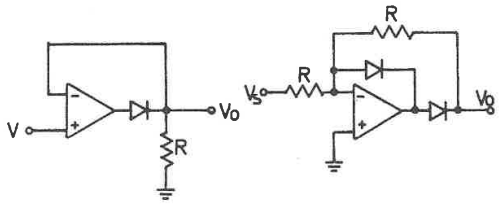


a) b)

Fig. 3.67 Peak detectors: a) passive, b) active (output is for $V_i=V_p \sin\omega t$).

T4. Active half-wave rectifier:

Similar to the case of active peak detectors, active half-wave rectifiers are more precise compared to the conventional half-wave rectifiers. If the input signal applied to a passive half-wave rectifier is smaller than the diode barrier voltage, no output can be taken. But for active half-wave rectifier configurations, the effective value of barrier voltage is decreased to μV ranges as explained in T3. In this case, voltages comparable with the barrier voltage can be rectified with a minimum distortion. Two possible active half-wave rectifiers are shown in Fig. 3.68. It is also possible to design similar active full-wave rectifier circuits having similar specifications.



a) b)

Fig. 3.68 Active half-wave rectifiers with a) one diode, b) two diodes.

T5. Active positive limiter (clipper) and clamper:

Similar to the active diode circuits given in T3 and T4, the restrictions stemming from the diode barrier voltage in passive limiter circuits are overcome using active limiter circuits. An example of active positive limiter is shown in Fig. 3.69. It is also possible to design an active clamper circuit as shown in Fig. 3.70.

PRELIMINARY:

P1. Verify the V_o equations given for integrator and differentiator circuits.

P2. Explain the operation of the active diode circuits given in T3, T4 and T5 and compare with the corresponding passive circuits.

P3. Design an active full-wave rectifier circuit with the help of the active half-wave rectifier circuits given in Fig. 3.68.

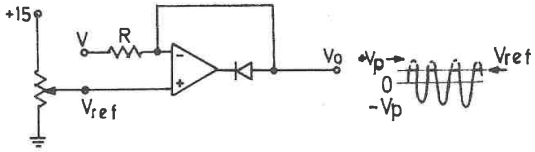


Fig. 3.69 Active clipper (output is for $V_i=V_p\sin\omega t$).

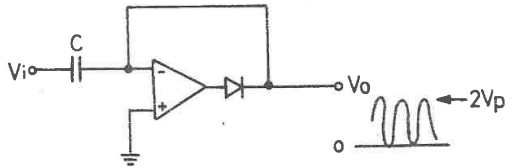


Fig. 3.70 Active clamper (output is for $V_i=V_p\sin\omega t$).

EXPERIMENTAL PROCEDURE:

■ Use R=10 K, C=0.1 μF and 5 K pot throughout the procedure. Measure the input and output voltages with CRO.

E1. Connect the circuit of Fig. 3.66a with V_i=4 $V_{p\text{-}p}$ square wave at 100 Hz. Draw V_i and V_o on the same scale.

E2. Connect the circuit of Fig. 3.66b with V_i=4 $V_{p\text{-}p}$ triangular wave at 100 Hz. Draw V_i and V_o on the same scale.

E3. Connect the circuit of Fig. 3.67b. Draw V_i and V_o on the same scale for:

a) V_i=(4sinωt) V at 100 Hz,

b) V_i=(0.5sinωt) V at 100 Hz.

E4. Connect the circuit of Fig. 3.68a. Repeat the procedure E3.

E5. Connect the circuit of Fig. 3.68b. Repeat the procedure E3.

E6. Connect the circuit of Fig. 3.69. Take V_i=(4sinωt) V at 100 Hz and V_{ref} =2 V. Observe and draw V_i and V_o on the same scale.

E7. Connect the circuit of Fig. 3.70 with V_i=(4sinωt) V at 100 Hz. Draw V_i and V_o on the same scale.

CONCLUSIONS:

C1. Compare the experimental and theoretical results. Comment on the differences between them if exist.

C2. Compare the results of the two active half-wave rectifier circuits given in Fig. 3.68, and experimented in E4 and E5.

EQUIPMENT LIST:

Resistors (2*10 K)Ω

Potentiometer (5 K)Ω

Capacitor (0.1/500 V)μF

Rectifier diodes (2*1N4001)

IC OPAMP (LM741)

Standard set equipment.

EXPERIMENT

16

AUDIO POWER AMPLIFIERS

OBJECTIVE:

To become familiar with audio power amplifiers and to examine their working principles.

THEORY:

T1. Classification of amplifiers:

Due to efficiency considerations, the active devices used in power amplifiers are so biased that they are cut off for certain intervals of time. This interval may generally be a fraction of the incoming signal and is defined as **conduction angle**, the ratio of the duration of the operation of the active device to the period of the incoming signal. Consider a sinusoidally varying input (one period of a sinusoidal wave corresponds to 360° conduction angle). According to this input, transistor amplifiers can be classified as:

class A 360° conduction angle,

class B 180° conduction angle,

class AB 180° < conduction angle <360°,

class C conduction angle <180°,

class D no conduction angle is defined (switched operation).

In this experiment, class A, B and AB types will be studied.

One of the most important parameters of the power amplification is the **efficiency** η which is defined as the ratio of the usable amplified AC power to the total power consumed by the output stage. A higher efficiency corresponds to less waste power dissipation.

When dealing with power calculations of different amplifier configurations, let us use the symbols given below:

P_S : Supply power (i.e. input power from supply)

P_L : AC power delivered to load

P_{Ldc} : DC power delivered to the load, other resistors and bias network

P_D : Power dissipated in the device (i.e. at collector junction)

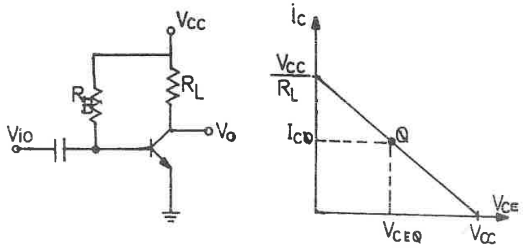
These power terms can be related as,

$$P_S = P_L + P_{Ldc} + P_D$$

According to the definition, efficiency can be written as,

$$\eta = \frac{P_L}{P_S} \times 100\ (\%)$$

T2. Class A type amplifiers:



a) b)

Fig. 3.71 a) Class A direct coupled amplifier, b) load line.

The simplest class A amplifier configuration is shown in Fig. 3.71a. The operating point is placed at the linear portion of the output characteristics as shown in Fig. 3.71b. In this case, the power relations can be written as

$$P_L = \frac{I_{cm}^2}{2} R_L$$

$$P_{Ldc} = I_{CQ}^2 R_L$$

$$P_S = V_{CC} I_{CQ}$$

$$P_D = P_S - P_L - P_{Ldc}$$

where I_{cm} is the maximum value of the AC portion of the collector current. For the maximum symmetrical swing at the output, it is evident from the load line that

$$I_{cm} = I_{CQ} = \frac{V_{CC}}{2 R_L}$$

Putting I_{cm} and I_{CQ} in P_L and P_S gives,

$$P_{L(max)} = \frac{V_{CC}^2}{8 R_L} \quad , \quad P_S = \frac{V_{CC}^2}{2 R_L}$$

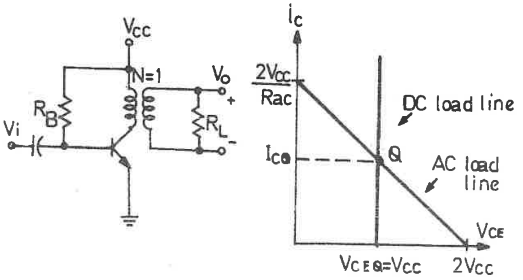
This yields a maximum efficiency $\eta_{(max)}$ of 25 % which is very low in fact.

In order to increase the efficiency of class A type amplifiers, P_{Ldc} must be eliminated. One way of doing this is to use transformer coupling as shown in Fig. 3.72a. In this case, inductor behaves as short circuit on DC conditions and Q point is placed at $V_{CEQ}=V_{CC}$, if the primary resistance of the transformer is ignored. The effective dynamic load seen from the collector can be written as,

$$R_{ac} = N^2 R_L$$

where N is the transformer's turn ratio N_1/N_2. In this case, the DC and AC load lines are not coincident and AC load line has a slop of $-1/R_{ac}$ as

shown in Fig. 3.72b. The power relations for this type transformer coupled class A power amplifiers can be written as (omitting transformer's primary resistance),



a) b)

Fig. 3.72 a) Class A transformer coupled amplifier, b) load line.

$$P_L = \frac{I_{cm}^2}{2} R_{ac}$$

$$P_S = V_{CC} I_{CQ}$$

$$P_D = P_S - P_L$$

and P_{Ldc}=0, since there is no DC voltage drop across the primary side of the transformer. For the maximum symmetrical swing at the output,

$$I_{cm} = I_{CQ} = \frac{V_{CC}}{R_{ac}}$$

from Fig. 3.72b. Putting these values leads

$$P_{L(max)} = \frac{V_{CC}^2}{2\ R_{ac}} \quad , \quad P_S = \frac{V_{CC}^2}{R_{ac}}$$

and a maximum efficiency $\eta_{(max)}$ of 50 % which shows that the transformer coupled class A stage is twice efficient than the direct coupled class A power amplifier.

T3. Class B type amplifiers:

Since a transistor conducts only 180° of input signal in class B operation, two transistors are needed to conduct the whole input signal. The simplest class B configuration is given in Fig. 3.73a. This amplifier is composed of a pair of emitter followers of one npn and one pnp transistors, and the load is directly coupled to the active devices. Normally, when no input signal is present, transistors are at cutoff and no DC current flows through the load. For a positive input of $V_i > V_\gamma$, T1 will be active and amplifies the positive input signal while T2 remains off. Similarly, when $V_i < -V_\gamma$, T2 conducts and T1 remains off. In this way, an input signal of $-V_\gamma > V_i > V_\gamma$, can be amplified, but the part $|V_i| < V_\gamma$ can not. This unamplified portion of the input signal causes

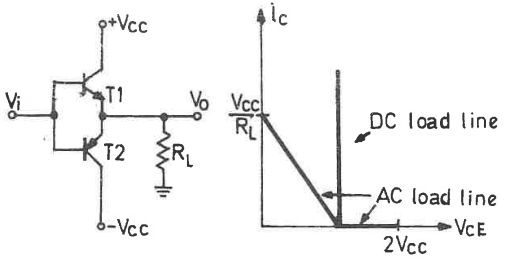
crossover distortion at the output, which is the main disadvantage of the class B configuration.

The power relations for a direct coupled emitter follower class B power amplifier can be written as,

$$P_L = \frac{I_{cm}^2}{2} R_L$$

$$P_S = \frac{2\, I_{cm}}{\pi} V_{CC}$$

$$2\, P_D = P_S - P_L$$



a) b)

Fig. 3.73 a) Class B direct coupled amplifier, b) load line for one of the transistors.

For the maximum symmetrical swing at the output, each transistor must be operated at

$$I_{cm} = I_{CQ} = \frac{V_{CC}}{R_L}$$

as shown in Fig. 3.73b. In this case, the maximum load power and the source power can be written as,

$$P_{L(max)} = \frac{V_{CC}^2}{2\, R_L} \quad , \quad P_S = \frac{2}{\pi} \frac{V_{CC}^2}{R_L}$$

These values lead a maximum achievable efficiency $\eta_{(max)}$=78.5%.

The disadvantage of the direct coupled class B configuration is the low voltage gain (less than unity) due to emitter follower configuration employed. If a higher voltage gain is desired, the load can be coupled via transformer as shown in Fig. 3.74. In this case, the effective value of the dynamic load seen from the collector is,

$$R_{ac} = N^2\, R_L$$

and the power relations given for direct coupled amplifier are valid if R_L in these relations is replaced with R_{ac}. It should be kept in mind that there is still crossover distortion at the output.

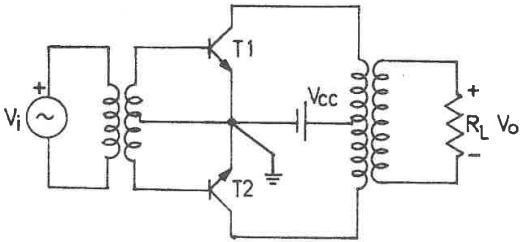


Fig. 3.74 Class B transformer coupled amplifier.

T4. Class AB type amplifiers:

As mentioned in T2, class A direct coupled amplifiers consume power even if the input signal is not present. This disadvantage is eliminated in class B types at the expense of the crossover distortion due to the unamplified portion of the input signal. In order to eliminate the crossover distortion in class B types, the class AB type amplifiers are introduced. In this type, the transistors are biased just at the threshold of conduction so that they consume as less power as possible at no load condition. Class AB type power amplifiers can be in the form of direct coupled as in Fig. 3.75 or transformer coupled as in Fig. 3.76. Direct coupled class AB amplifiers have low voltage gain and high current gain whereas transformer coupled ones have high current and voltage gain.

The transistors, in this configuration, are biased in a way that the voltage drop on R_2 is adjusted to be approximately equal to V_γ in this type.

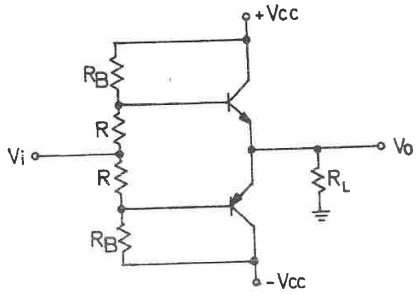


Fig. 3.75 Class AB direct coupled amplifier.

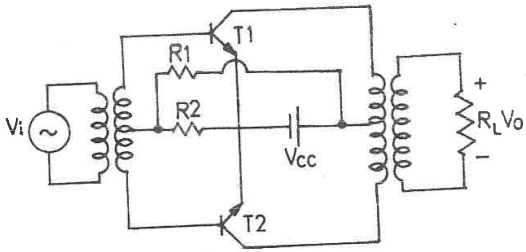


Fig. 3.76 Class AB transformer coupled amplifier.

The class AB operation results in less distortion than class B, but the price that must be paid for this improvement is a reduction in efficiency and waste of standby power (i.e. no input power).

T5. Practical considerations:

The amplifier configurations mentioned so far are not practical in fact, but they are given to make calculations simpler and to provide better understanding. In real amplifiers, however, stability, frequency response, source resistance, transformer winding resistances etc. all must be taken into account. The amplifier configurations given in the experimental procedure include emitter resistors for stability and input and output capacitors for DC blocking. The supply voltages for all amplifier types may be chosen to be single or dual according to design specifications. Dual supply designs are better since the symmetry is provided by the sources, but if single supply is used in class B or AB types, the circuit must be redesigned (i.e. for example, resistors must be chosen) to be operated symmetrically.

PRELIMINARY:

■ Assume that $|V_{BE}|$=0.65 V and β=120 for all transistors used in this experiment (use these values for the calculations carried out in preliminary).

P1. Given that R_L=100Ω, R_2=1 K and V_{CC}=12 V for the circuit of Fig. 3.77.

a) Calculate the value of R_1 so that the maximum output voltage swing can occur. Also calculate the DC power consumed on each resistor.

b) Calculate $A_V=V_o/V_i$.

c) Calculate P_S, P_{Ldc} and the maximum value of P_D if no input signal is present.

d) Calculate the P_L and P_D when $V_i=(20\sin\omega t)$mV. Hint: Use the result of P1b to find I_{cm}.

P2. Given that V_{CC}=6 V for the circuit given in Fig. 3.78.

a)Calculate the minimum value of R_L such that the peak collector current is less than 55 mA (take V_{CEsat}=0).

b) Assuming that $V_i=(2\sin\omega t)$ V, draw the input and output voltage waveforms on the same scale.

P3. Calculate the value of R to give a standby collector current of 12 mA for the circuit given in Fig. 3.79. Also calculate V_{CEQ} for each transistor.

EXPERIMENTAL PROCEDURE:

■ Test your BJTs using DMM in KΩ range.

■ Use C_i=22 μF, C_o= 220 μF whenever needed.

■ Set the frequency of SG to 1 KHz.

E1. Connect the circuit of Fig. 3.77 with the values given and calculated in P1.

a) Measure I_{CQ} and V_{CEQ} and compare the measured values with

the theoretical ones calculated in P1. If there is a big difference between the calculated and measured V_{CEQ} values, use the 10 K pot to overcome this problem (i.e. to set V_{CEQ}=6 V).

b) Using the low output (LO) of the signal generator, adjust V_i=(100sinωt)mV. Measure V_i and V_o on the CRO and increase the input voltage until the maximum undistorted output signal is obtained (i.e. the output must remain sinusoidal since the input is sinusoidal). Record the values of V_i and V_o and calculate the voltage gain (V_o/V_i) at the maximum output voltage swing position.

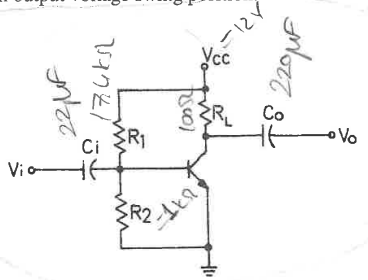


Fig. 3.77 Experimental class A direct coupled amplifier.

E2. Connect the circuit of Fig. 3.78 with the values given and calculated in P2.

a) Adjust V_i=(1sinωt) V. Measure V_i and V_o on CRO and increase the input voltage until the maximum undistorted output signal is obtained. Observe the crossover distortion at the output.

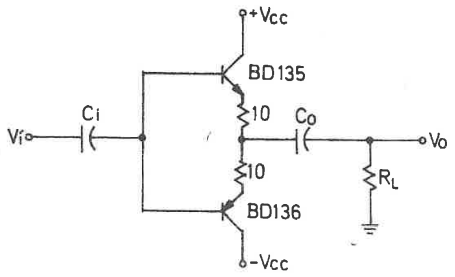


Fig. 3.78 Experimental class B direct coupled amplifier.

b) Record the output voltage values corresponding to the input signals of (2sinωt) V and (6sinωt) V, respectively. Find a relation between the input and output voltages.

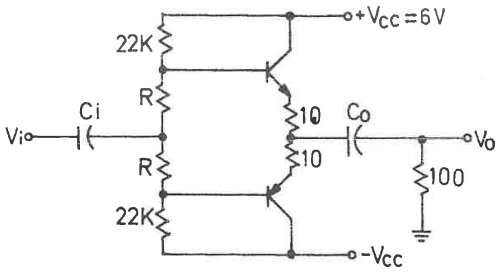


Fig. 3.79 Experimental class AB direct coupled amplifier.

E3. Connect the circuit of Fig. 3.79 with the values given and calculated in P3.

a) Measure I_{CQ} and V_{CEQ} and compare the measured values with the theoretical calculated in P3.

b) Adjust V_i=(1sinωt) V. Measure V_i and V_o on the CRO and increase the input voltage until the maximum undistorted output signal is obtained.

c) Record the output voltage values corresponding to the input signals of (2sinωt) V and (6sinωt) V, respectively. Find a relation between the input and output voltages.

CONCLUSIONS:

C1. Compare the distortion and voltage gain results for class B and class AB type amplifiers.

EQUIPMENT LIST:

Resistors (2*10/5W, 100/5W, 1 K, 2*5.6 K, 10 K, 2*22K)Ω

Potentiometer (10 K)Ω

Capacitors (22/16V, 220/16V)μF

BJT (BD135-npn, BD136-pnp)

Standard set equipment.

EXPERIMENT

17

REGULATED POWER SUPPLIES

OBJECTIVE:

To experiment the transistor and the three terminal IC voltage regulators. To investigate the effects of changing load and varying line voltage.

THEORY:

T1. Load and line regulation:

The percent load and line regulation quantities described below show how good the regulator is. Ideally, both the load and line regulation of a power supply must be zero. This means that, the output voltage of a regulator is independent of the value of the load connected, and the variations in the input voltage. However, this is not the case for practical voltage regulators.

The load regulation is calculated using DC quantities as

$$\%\ load\ regulation = \frac{V_{L(nl)} - V_{L(fl)}}{V_{L(nl)}} \times 100$$

where $V_{L(nl)}$ and $V_{L(fl)}$ are the no load and full load output voltages, respectively.

The line regulation is calculated using AC quantities as

$$\%\ line\ regulation = \frac{\Delta V_o}{\Delta V_i} \times 100$$

where ΔV_i is the change in the input voltage of the regulator and ΔV_o is the change in the output voltage caused by ΔV_i.

T2. Zener diode regulator:

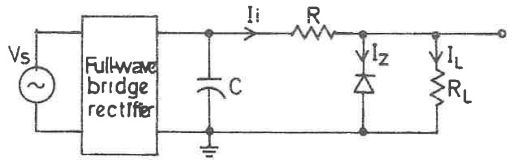
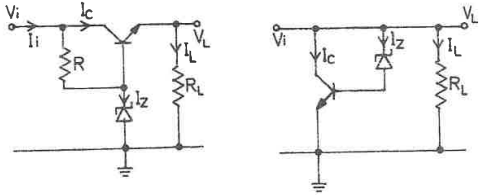


Fig. 3.80 Zener diode regulator.

The simplest voltage regulator is the zener diode regulator shown in Fig. 3.80. The limitation on the performance of this configuration is

the effect of changing R_L (or I_L). Since $I_i=I_L+I_Z$, a change in the load current produces an equal but opposite change in the zener current ($\Delta I_L=-\Delta I_Z$). The changes in the zener current will result in a change in the output voltage since the voltage drop on r_Z will be changed. This is because $V_o \simeq V_Z$ if $V_i > V_Z$.

T3. Transistor series regulator:



a) b)

Fig. 3.81 Transistor voltage regulators: a) series, b) shunt.

The simplest way to increase the current handling capacity of a zener diode regulator is to add an emitter follower as shown in Fig. 3.81a. In this case,

$$V_o = V_Z - V_{BE}$$

but the change in the zener current is reduced by a factor of $\beta+1$, i.e.

$$\Delta I_L = -(\beta + 1)\Delta I_Z$$

This regulator is called as the **series regulator** since the transistor is connected in series between the input and output. The operation of the series regulator can be explained as follows:

$$R_L \downarrow \quad V_o \downarrow \quad I_L \uparrow \quad I_B \uparrow \quad V_{CE} \downarrow \quad V_o \uparrow$$

The other simple transistor regulator is the **shunt regulator** shown in Fig. 3.81b. This regulator is not as commonly used as series regulator, since the maximum collector current flows through the transistor at no load.

T4. Series regulator with negative feedback:

A series regulator with negative feedback is shown in Fig. 3.82. In this configuration, Q2 acts as an emitter follower and Q1 provides the voltage gain in a negative feedback loop. The output voltage is almost kept constant across the changes in R_L by the following way:

$$R_L \downarrow \quad V_o \downarrow \quad I_L \uparrow \quad V_F \downarrow \quad I_{C1} \downarrow \quad I_B \uparrow \quad V_{CE} \downarrow \quad V_o \uparrow$$

The output voltage can be written as

$$V_F = V_Z + V_{BE1} = \frac{V_o}{R_2 + R_1} R_1$$

$$V_o = \frac{R_2 + R_1}{R_1} (V_Z + V_{BE1})$$

The potentiometer in the circuit is used for adjusting the output voltage to a specific value.

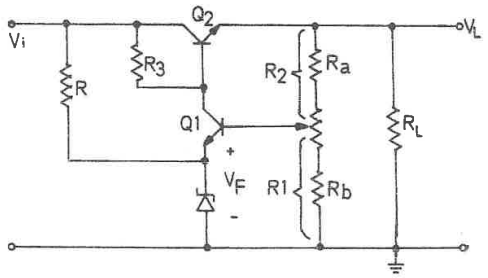


Fig. 3.82 Series regulator with negative feedback.

T5. Current limiting and short circuit protection:

If accidentally a short circuit takes place at the output of the series regulator shown in Fig. 3.82, an enormous current flow through Q2 which can destroy either Q2 or one of the diodes in the bridge rectifier. In order to avoid this harmful effect, another transistor Q3 and a resistor

R_4 are placed in the series regulator circuit as shown in Fig. 3.83.

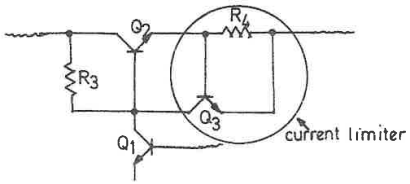


Fig. 3.83 Current limiting for the series regulator with negative feedback.

The resistor R_4 is chosen so that $I_{E2} \cdot R_4 < V_{BE3}$ in normal operation. If I_{E2} increases enormously, $I_{E2} \cdot R_4 \geq V_{BE3}$. In this case Q3 turns on and I_{C3} flows through R_3. This process result in decreasing V_{B2} and V_o to prevent any circuit component from damage. For example, if we want to limit the output current to 100 mA and V_{BE3} is 0.7 V, R_4 must be 0.7 V/100 mA=7 Ω.

It is also possible to add some other components to the series regulator to protect the parts from thermal runaway. But this requires complex circuitry and big construction areas to build.

T6. Three-terminal IC regulators:

The second generation IC regulators generally have a built-in short circuit protection and thermal shutdown in a small composite device. The output of this type of regulators can be adjusted over wide

ranges with a few external components. These IC regulators can drive load currents of 0.1 to 3 A, typically.

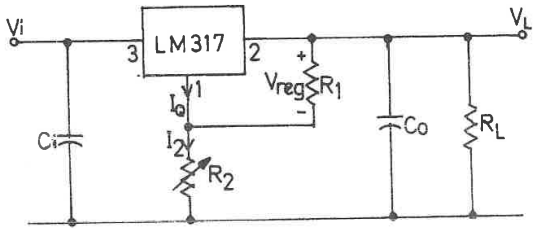


Fig. 3.84 LM317 application circuit (C_i and C_o are optional).

LM317 is a second generation adjustable voltage regulator with the following specifications:

I_o max. 1.5 A

V_o typically. 1.25-37 V

V_i typically. 3-40 V

load regulation typically. 0.1%

line regulation typically. 0.01%

A typical adjustable voltage application of LM317 is shown in Fig. 3.84, where,

$$I_2 = \left(\frac{V_{reg}}{R_1} + I_Q \right)$$

$$V_L = V_{reg} + I_2 R_2$$

and if I_Q is neglected (which is in nA range),

$$V_L = V_{reg} \left(1 + \frac{R_2}{R_1} \right)$$

There are also constant voltage IC regulators such as 78XX and 79XX series. The first two digits in the code show the type of the regulator and the last two digits show the voltage value. For instance, 7805 is a 5 V positive voltage regulator whereas 7912 is a 12 V negative voltage regulator. These types are not examined in this experiment.

PRELIMINARY:

P1. Explain the operation of the circuits given in the Theory section.

EXPERIMENTAL PROCEDURE:

■ Measure V_L at the DC mode of the CRO and $V_{Cripple}$ and $V_{Lripple}$ at the AC mode.

E1. Connect the circuit of Fig. 3.85. Use 5 K pot to adjust the maximum and the minimum values of V_o. Fill in the Table 3.6.

E2. Connect the circuit of Fig. 3.86 with C=470 μF, C_i=100 nF and C_o=1

μF. Use 5 K pot to adjust the maximum and the minimum values of V_o. Fill in the Table 3.7.

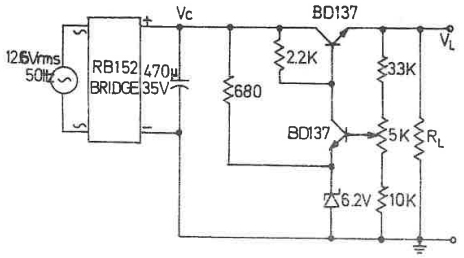


Fig. 3.85 Experimental transistor series voltage regulator.

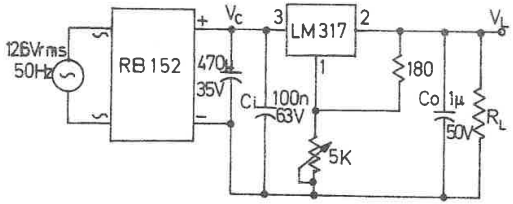


Fig. 3.86 Experimental IC voltage regulator.

R_L (Ω)	$V_{L(max)}$ (V)	$V_{L(min)}$ (V)	$V_{C\ ripple}$ (mV_{p-p})	$V_{L\ ripple}$ (mV_{p-p})
∞ (open)		X		
∞ (open)	X			
270		X		
270	X			

V_L (V)	R_L (Ω)		
12	∞		
12	270		

Table 3.6 Data obtained at E1.

R_L (Ω)	$V_{L(max)}$ (V)	$V_{L(min)}$ (V)	$V_{C\ ripple}$ (mV_{p-p})	$V_{L\ ripple}$ (mV_{p-p})
∞ (open)		X		
∞ (open)	X			
270		X		
270	X			
270 (no C_i, C_o)		X		
270 (no C_i, C_o)	X			

V_L (V)	R_L (Ω)		
12	∞		
12	270		

Table 3.7 Data obtained at E2.

CONCLUSIONS:

C1. Compare the experimental and theoretical results. Comment on the differences between them if exist.

C2. Calculate the load regulations for the maximum and minimum values of V_L for both the series regulator and IC regulator circuits. Compare the results.

EQUIPMENT LIST:

Resistors (180, 270/0.5 W, 680, 2.2. K, 3.3 K, 10 K)Ω.

Potentiometer (5 K)Ω

Capacitors (470/35 V, 1/50 V)μF and 100 nF/63 V

Bridge rectifier (RB152)

Zener diode [BZX8506V2 (6.2 V)]

Transistors (2*BD137 npn)

IC regulator (LM317)

Standard set equipment.

CHAPTER 4

COMPONENTS USED IN THE EXPERIMENTS

4.1. RESISTORS, POTENTIOMETERS AND RESISTANCE DECADE BOX

Resistors:

The resistors with 4 color codes and 10% tolerances are used throughout the experiments in this manual. However one can find the resistors with 5 or 6 color bands with higher precision.

Carbon resistors of 10 percent are avaliable in power ratings of 1/4, 1/2, 1 and 2 W in the following range:

2.7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2, 10, 12, 15, 18, 22

with all 10^n multiples, n ranging from 0 to 6.

The most commonly used type, 4 color band resistor, is shown in Fig. 4.1.

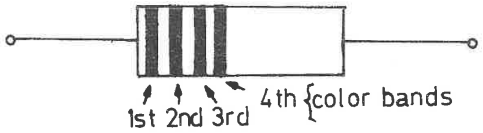


Fig. 4.1 Resistor color codes.

The resistor color codes can be used to read the resistor values using the following guide:

1st band	gives the 1st digit
2nd band	gives the 2nd digit
3rd band	gives the number of zeros to following the 2nd digit (n of $*10^n$)
4th band	gives ±% tolerance factor 20 if it is empty (no band) 10 if it is silver band 5 if it is gold band

Equivalent numbers of Color Codes:

0	Black
1	Brawn
2	Red
3	Orange
4	Yellow
5	Green
6	Blue
7	Violet
8	Gray
9	White

Potentiometers:

Typical values of potentiometers are the same as that of resistor's. But generally they have found in market having values like 500 Ω, 1KΩ, 5KΩ, 10 KΩ, 100 KΩ etc. The most common potentiometers in the market are in the shape given in Fig. 4.2 with the center lead

corresponding to the adjustable pointer.

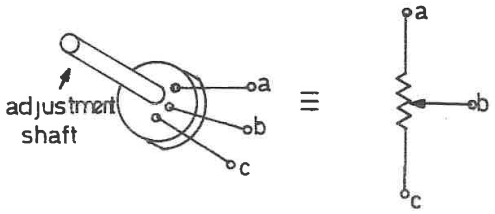


Fig. 4.2 A typical potentiometer and its circuit equivalent.

Resistance Decade Box:

Resistance decade box is a device which can be used to obtain any resistance values between 1 to 99999 Ω with 1 Ω steps (the range and steps may be different for different types of decade boxes). When used as a load, its "decade" terminals must be connected to the circuit.

4.2. CAPACITORS

Various types of electrolytic capacitors can be found in the market. They are typically found in the shapes given in Fig. 4.3 and generally their negative terminals are marked by the manufacturers.

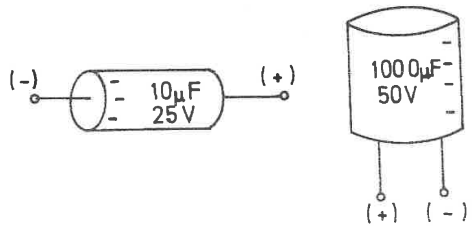


Fig. 4.3 Typical capacitor shapes.

4.3. DIODES AND OPTOELECTRONIC DEVICES

Rectifier diode: (1N4001) I_{max}=1 A, $V_{r\,max}$<50 V

Scheme for a typical rectifier is given in Fig. 4.4.

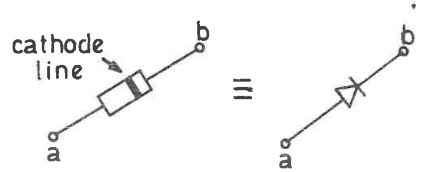


Fig. 4.4 A typical low power rectifier diode.

Zener diode: (BZX8506V2) V_z=6.2 V, $P_{D\,max}$=200 mW

Scheme for a typical zener diode is given in Fig. 4.5.

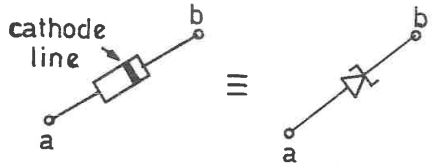


Fig. 4.5 A typical zener diode.

Light Emitting Diode: (MV5353, TIL221, and TIL222)

I_f=35-50 mA, $V_{r\,max}$ < 5V

Scheme for two typical LED types and their circuit equivalent are given in Fig. 4.6.

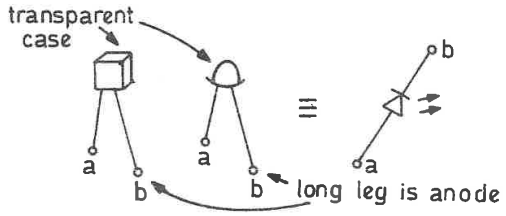


Fig. 4.6 Typical LEDs and circuit equivalent.

Bridge diode: (RB152) I_{max}=3 A, $V_{r\,max}$<50 V

Lead configuration for RB152 is given below:

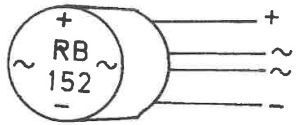


Fig. 4.7 RB152 bridge diode.

Seven segment display: (SEL620 or TIL312)

Lead configuration for SEL620 is given in Fig. 4.8.

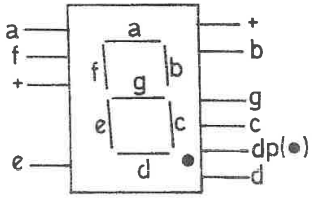


Fig. 4.8 Lead configuration of SEL620 7-segment display.

Optocoupler: (4N26 or 4N27)

Lead configuration for 4N26 is given in Fig. 4.9.

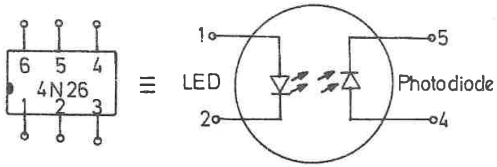
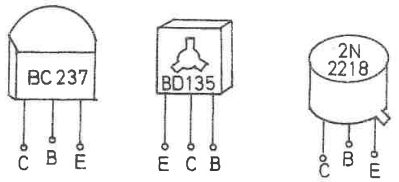


Fig. 4.9 4N26 optocoupler pin diagram.

4.4. TRANSISTORS

BJTs:

Code	Type	lead type	V_{CEo}/ V_{EBo} (V)	I_C (A)	β	P_{tot} (W)	BW (MHz)
BC237	npn	1	50/6	0.1	120-460	0.3	>150
BD135	npn	2	45/5	1.5	40-250	12.5	250
BD136	pnp	2	45/5	1.5	40-250	12.5	75
BD137	npn	2	60/5	1.5	40-160	12.5	250
2N2218	npn	3	80/6	1	>40	1	250



type 1 *type 2* *type 3*

Fig. 4.10 Typical BJT cases and lead configuration types.

JFET: (BF245) $I_{DSS} > 10$ mA, $V_p < 14.5$ V

Case of BF245 is similar to the BJT type 1. C, B, E in this figure will be replaced with G, S and D, respectively.

4.5. INTEGRATED CIRCUITS

Linear Operational Amplifier: (LM741)

The pin diagram for LM741 OPAMP is given in Fig. 4.11.

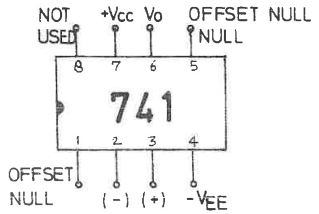


Fig. 4.11 LM741 pin diagram.

The specifications of LM741 given by the manufacturer are:

A_{OL}	20-200 V/mV (R_L>2KΩ , Vo=±10 V) (open loop gain)
R_i	0.3-2 MΩ (input resistance)
R_o	typically 75 (output resistance)
I_B	typically 80 max 500 nA (input bias current)
V_{io}	typically 1 max 6 mV (Rs=10 KΩ)
I_{io}	typically 20 nA (input offset current)
CMRR	typically 30000 (common-mode rejection ratio)
PSRR	typically 10 max 150 μV/V (power supply rejection ratio)
V_{CC}, $-V_{EE}$	max +18 V (supply voltage)
V_i	max ±13 V (input voltage)

V_o	max ±13 V (output voltage)
I_{osc}	typically 25 mA (output short circuit current)
I_{CC}	typically 1.4 max 2.8 mA (supply current)
P_D	typically 50 max 85 mW (dissipated power)

Variable Voltage Regulator: (LM317)

LM317 is a typical second generation adjustable voltage regulator with the following specifications:

I_o	max. 1.5 A
V_o	typ. 1.25-37 V
V_i	typ. 3-40 V
load regulation	typ. 0.1%
line regulation	typ. 0.01%

The pin diagram for LM317 is given in Fig. 4.12.

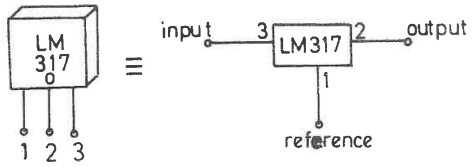


Fig. 4.12 LM317 variable voltage regulator pin diagram.

APPENDIX

PART

REQUIREMENTS

The following part list must be present in a laboratory where all the experiments given in this manual are performed.

A.1. RESISTORS, POTENTIOMETERS AND RESISTANCE DECADE BOX

Resistors:

Resistance (Ω)	Quantity	Wattage (Watts)	Resistance (Ω)	Quantity	Wattage (Watts)
10	2	5	1.8K	1	0.25
10	1	0.5	2.2K	1	0.25
56	1	0.5	2.7K	3	0.25
68	1	0.5	3.3K	1	0.25
100	1	5	5.6K	2	0.25
100	2	0.25	10K	4	0.25
150	1	0.25	12K	1	0.25
180	1	0.25	15K	1	0.25
270	1	0.5	18K	1	0.25
270	2	0.25	22K	2	0.25
470	1	0.25	56K	1	0.25
680	1	0.25	100K	2	0.25
1K	2	0.25	11M	2	0.25
1.5K	2	0.25			

Table A.1 Resistor requirements.

Potentiometers: One from each (all 2 W):

470 Ω, 5 KΩ, 10 KΩ, 47 KΩ

Resistance Decade Box: One, adjustable from 1 to 99999 Ω with 1 Ω steps.

A.2. CAPACITORS

Capacitance (μF)	Quantity	Voltage (Volts)	Capacitance (μF)	Quantity	Voltage (Volts)
100 nF	1	63	100	2	25
0.1	1	500	220	1	25
1	1	50	470	1	35
10	1	16	2200	1	25
22	1	25			

Table A.2 Capacitor requirements.

A.3. DIODES AND OPTOELECTRONIC DEVICES

One from each unless stated:

Rectifiers: 4*1N4001

Bridge rectifier: RB152

Zener: BZX8506V2

LEDs: MV5353, TIL221, TIL222

Seven segment display: SEL620 or TIL312

Optocoupler: 4N26 or 4N27

A.4. TRANSITORS

One from each unless stated:

BJTs:	3*BC237	npn
	BD135	npn
	BD136	pnp
	2*BD137	npn
	2N2218	npn
JFET:	BF245	n-channel

A.5. INTEGRATED CIRCUITS

One from each:

Operational Amplifier: LM741

Variable Voltage regulator: LM317

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