**UNIVERSITY OF GAZIANTEP**

**ELECTRICAL AND ELECTRONICS ENGINEERING DEPARTMENT**

**EEE 340 DIGITAL DESIGN I**

**LABORATORY EXPERIMENT - 3**

**FPGA IMPLEMENTATION OF BASIC LOGIC CIRCUITS I**

**1. OBJECT**

In this experiment you will implement some basic logic gates and circuits on FPGA by using Verilog HDL and synthesizer.

**2. EXPERIMENTAL WORK**

**E1**. Write the Verilog code for 2-input AND Gate, 3-input NAND Gate and 4-input OR Gate.When you complete your design, synthesize it and have your circuit verified by lab instructor.

**E2**. Design the circuit given below using Verilog. Obtain its truth table. When you completeyour design, have your circuit verified by lab instructor.



 A

 B

 C

 D

*Note:* Your module structure must be like this:

module Lab1\_E2(

input A,

input B,

input C,

input D,

output E

);

**E3.** Simulate and verify the circuit you have designed in E2 using provided testbench file. If your design passes the test, add the necessary UCF file to your design and load your circuit onto FPGA using Digilent Adept software.

**Caution:** *The FPGA boards contain many exposed components that are sensitive to static**electricity. Before touching the boards, try to remember to discharge any static electricity you may have built up by touching a grounded piece of metal. Also please hold the board from the sides when you have to and avoid touching exposed components on the board.*

**3. TESTBENCH**

`timescale 1ns / 1ps

module E2\_tb;

 parameter finishtime = 10;

 integer N;

 // Inputs

 reg [3:0] test\_vector;

 // Outputs

 wire E;

 // Instantiate the Unit Under Test (UUT)

 Lab1\_E2 uut (

 .A(test\_vector[3]),

 .B(test\_vector[2]),

 .C(test\_vector[1]),

 .D(test\_vector[0]),

 .E(E)

 );

 initial begin

 // Initialize Inputs

 $monitor ("TIME = %d, test\_vectors = %b, E = %b", $time, test\_vector, E);

 test\_vector = 4'b0000;

 end

 initial begin

 for(N=0; N<16; N=N+1) begin

 #5 test\_vector = (test\_vector + 1'b1);

 #1

 if (E == ~((test\_vector[3] & test\_vector[2]) & (test\_vector[1] | test\_vector[0]))) $display ("PASS");

 else $display ("FAIL");

 end

 #finishtime // everything below will printout after "finishtime"

 $display ("Finishing simulation");

 $display ("Time is - %d",$time);

 $finish;

 end

endmodule

**4. FPGA PIN NUMBERS**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Logical PIN Name** | **Hardware on the Board** |  | **FPGA PIN** |  |
|  |  |
|  |  |  |  |  |
| S1 | Switch 1 |  | A10 |  |
|  |  |  |  |  |
| S2 | Switch 2 |  | D14 |  |
|  |  |  |  |  |
| S3 | Switch 3 |  | C14 |  |
|  |  |  |  |  |
| S4 | Switch 4 |  | P15 |  |
|  |  |  |  |  |
| S5 | Switch 5 |  | P12 |  |
|  |  |  |  |  |
| S6 | Switch 6 |  | R5 |  |
|  |  |  |  |  |
| S7 | Switch 7 |  | T5 |  |
|  |  |  |  |  |
| S8 | Switch 8 |  | E4 |  |
|  |  |  |  |  |
| O1 | Led 1 |  | U18 |  |
|  |  |  |  |  |
| O2 | Led 2 |  | M14 |  |
|  |  |  |  |  |
| O3 | Led 3 |  | N14 |  |
|  |  |  |  |  |
| O4 | Led 4 |  | L14 |  |
|  |  |  |  |  |
| O5 | Led 5 |  | M13 |  |
|  |  |  |  |  |
| O6 | Led 6 |  | D4 |  |
|  |  |  |  |  |
| O7 | Led 7 |  | P16 |  |
|  |  |  |  |  |
| O8 | Led 8 |  | N12 |  |
|  |  |  |  |  |